Using a new knob

The design of ST's FD-SOI transistor is set to give analogue designers a new knob to tune parameters. By **Graham Pitcher**

The move to semiconductor manufacturing processes with ever smaller dimensions continues with undiminished enthusiasm, even though progress may not be as quick as some in the industry have been used to.

This move to smaller dimensions – known as More Moore – is good for digital circuitry, but not so good for analogue technology. Andreia Cathelin, a senior member of STMicroelectronics' technical staff, said: "We still want to pursue More Moore, but we also want to make it a high yield manufacturing process and one which can respond to performance requirements."

The company started to look for a new way forward a decade ago, when it concluded that things would become difficult beyond the 40nm node. "One of the things we started to look at," she continued, "was thin channel oxide structures." These could be built with planar structures or in 3D. While the latter approach has developed into FinFETs, the former has become ST's FD-SOI technology – fully depleted silicon on insulator.

"From the semiconductor physics perspective, the structures are similar," Cathelin explained, "and we found we could produce both. But we got a better yield and better use of resources from FD-SOI, so we decided to go with this at 28nm, although the channel actually measures 24nm."

But one of the big benefits of FD-SOI to those building SoCs – and, potentially, discrete components – is that it is 'analogue friendly'.

"I'm an analogue designer," Cathelin pointed out, "and started my career working with 2.4µm analogue transistors. Working at that node was good because you got gain from an integrated transistor; the transistor curves were the same as those we learned about at university. But the benefits degraded at the 130nm node.

"CMOS is optimised for digital circuitry," she explained, "and for speed. Analogue is often the poor relation in a VLSI CMOS process."

That's not to say analogue can't be used on leading edge processes. "Because analogue performance degrades, we have to put in place a lot of tuning – ways to cope with things. With FD-SOI, we can reclaim analogue transistor performance – and the reason is the thin oxide and active layers."

Cathelin said the bulk CMOS analogue transistor can be viewed as more like a controlled resistor. "With ultra thin box and body FD-SOI, we have total dielectric isolation with no channel doping. The transistor has no pocket implants for source and drain, so transistors can offer the same analogue gain as they did at 130nm, but with the advantages of a 28nm channel."

The FD-SOI transistor features an ultra thin insulator, beneath which is a second gate, or transistor body (see fig 1). Cathelin said: "The top gate will have a particular transconductance, or gm, but the second gate will have a transconductance of, say, gm/10. And we can do things with this arrangement." In fact, she uses the analogy of a 'knob'. "It's a new degree of freedom; a new 'knob' for analogue designers."

Because of the transistor's design, engineers have the ability to use body biasing. "It's something not available in other technologies," Cathelin noted. Whereas the body of a transistor manufactured using a bulk CMOS process can be biased by about 0.3V, the physics of the FD-SOI transistor allow it to be biased to +2V. "The V_t variation with respect to body voltage is steeper in FD-SOI," Cathelin explained, "and produces a V_t variation range of 250mV. This is unprecedented; bulk processes usually offer only tens of mV."

In the digital domain, biasing is used to provide a steady state variation in order to change transistor speed. In analogue, biasing is the 'knob' to which

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Photo: Alamy, Illustration: Phil Holmes

Cathelin refers. "Where tuning was used in the past to keep parameters constant, this will be achieved in the future through body biasing, controlled by active circuitry."

Cathelin noted the approaches needed to tune circuits had to be applied in the signal path and so interfered with the active signal by adding parasitics and impedance variable elements.

"When you wanted to increase the gain in order to change the linearity, you also changed the noise, the power consumption and so on in the wrong way," she explained.

"When you fixed one thing, you changed others. Now, with FD-SOI, these measures are not in the signal path, so they won't bring in parasitics. The device has good electronic performance with so much margin that, when you tune for one parameter, you won't affect the others."

In this way, architectures can be optimised to range from performance to ultra low power consumption.

"When you work at lower frequencies," Cathelin noted, "the 28nm mode provides a comfortable transistor transition frequency (f_T), so you can design L (transistor length) to be larger than L_{min} and so get better gain, matching performance and maintain process margins."

Cathelin is keen to point out that analogue design is all about margins. "It's not about designing in a centred process corner," she said. "It's about creating products that have to last for 10 years in a range of conditions. Because we are not working at L_{min} and because the 28nm node gives enough margin, the design will be more stable because we can work in an area where second order effects are not seen."

In her opinion, the benefits include intrinsic gain, better output conductance, lower noise, lower variability and less parasitic capacitance. "And better gain means fewer stages and lower power consumption."

If analogue designers do want to work at higher frequencies, they will have a better gm to work with, compared to 28nm bulk CMOS. "So the circuit will consume less power and bring better performance," she said. "And FD-SOI transistors have an f_T/f_{max} of more than 300GHz, which makes them comparable with bipolar transistors produced on a BiCMOS process."

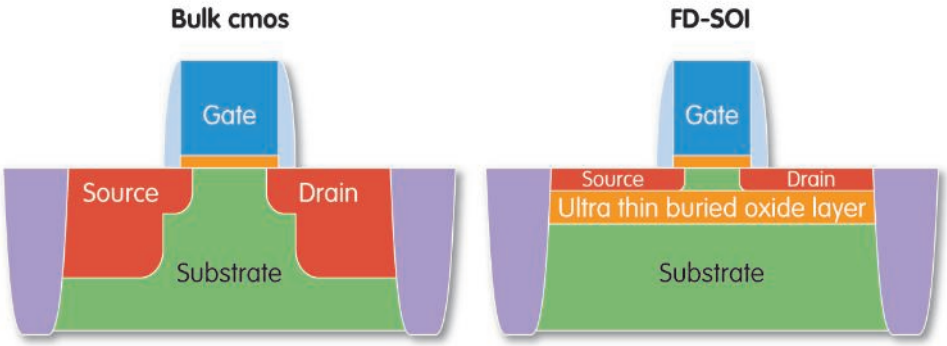

Fig 1: The FD-SOI transistor features an ultra thin insulator, beneath which is a second gate, or transistor body

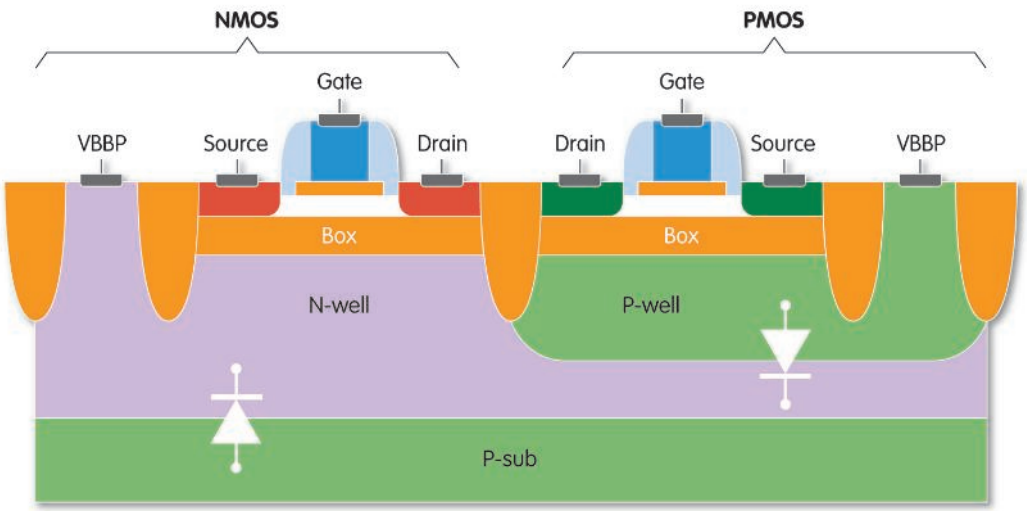

Fig 2: The 'flip well' process enables a large forward body bias range

Although FD-SOI is intended to support the manufacture of SoCs, it's not impossible to consider the process as being appropriate for the manufacture of discrete components, including data converters.

One of the reasons for this is switch performance. With better gate control and the ability to use back gate biasing, better quality analogue switches can be created. An indication of this is measuring the on resistance (R_{on}) of the pass gate with respect to input voltage. Cathelin said: "In regular CMOS, the ratio will be about 5:1 in the middle of the input voltage range. This makes things slower, so you need larger switches. With FD-SOI, the ratio at the same point is less than 2:1. So in a high speed data converter, for example, there could be benefits in speed and power consumption."

So, while FD-SOI might enable ultra low power SoCs for the IoT, it could also be used to create standard data converters.

Concluding, Cathelin said: "Analogue designers are happier; the transistor is back to offering good intrinsic performance and there is a 'knob' outside of the signal path. But if designers want to get the most out of FD-SOI, they will need to think about what they can do with that 'knob'."