Pointing to the future

Programmable platforms support moves to new comms interfaces.

By ***Roy Rubenstein.***

The need for ever greater traffic throughput in Ethernet switches and telecom equipment designs is forcing chip vendors to look beyond established interfaces such as the Optical Internetworking Forum's (OIF) System Packet Interface Level 4 (SPI-4.2) and the XAUI 10Gbit/s Ethernet interface. The picture, however, is far from clear.

"We have asked system vendors [about interfaces] and there are a number of in house implementations that are not standard," said Uday Mudoi, a strategic marketing manager at Vitesse. "We have tried to work with as many vendors as possible and hope the industry comes behind a standard, but we can't wait; we see a need now."

The larger equipment vendors favour proprietary interfaces – used, in part, to protect their designs from being easily replaced with competitors' equipment – alongside established standard interfaces.

The platform vendors are also considering emerging standards – such as the OIF's Scalable System Packet Interface (SPI-S) and Interlaken – that build on SPI-4.2 and are targeted at new technology standards such as 40Gbit/s and 100Gbit/s Ethernet. Interlaken, initially developed by Cisco Systems and Cortina Systems, is now backed by the Interlaken Alliance.

To add to the mix, another industry backed interface has emerged. Dubbed SPAUI, the interface is being proposed by fabless chip firm Dune Networks.

"From our perspective, SPAUI is one solution today – but not the only one," said Mudoi. "There is also double data rate XAUI supporting 6.25Gbit/s [per lane] which we support, but it is not a standard today."

Lattice and Altera are also supporting SPAUI. As fpga vendors, the two firms are well placed to help the industry transition to new high speed interfaces.

"Fortunately for us, network processors don't talk directly to carrier Ethernet switches," said Shakeel Peera, Lattice's director of strategic marketing for high performance fpgas.

Network processors (NPUs) use the SPI-4.2 interface, whilst Ethernet switches supporting 10Gbit/s interfaces use XAUI. "FPGAs and assps take up the bridging functionality from the NPU to the packet switch," said Peera.

Lattice is supporting SPAUI, despite it not being a standard, due to interest from tier one customers that have adopted Dune's switch fabric hardware. "SPAUI is not a mass standardisation interface," said Peera, "but we feel there is enough interest."

For Lattice, SPAUI collapses the best attributes of XAUI and SPI-4.2 within one interface. As a straight physical interface, XAUI has no packet flow control or traffic management when multiple packet types pass through the interface. "That is the role of the NPU and SPI-4.2, which deal with quality of service and flow control," said Peera.

SPAUI also uses far fewer pins, an important consideration for new ics that need multiple interfaces.

"SPI-4.2 uses 70 pins per interface and has a large logic implementation per chip" said Ori Aruj, senior director of marketing at Dune Networks. One, two or

even four SPI-4.2 interfaces are possible for a high throughput ic, but this would use 280 pins for the interfaces only. "That is the problem with SPI-4.2; it is a good interface, but complex to implement," said Aruj.

SPAUI, in contrast, uses 10 or 20% of the pins required for SPI-4.2 only, depending on the number of lanes. Like XAUI, SPAUI uses four lanes of data in a serialiser/deserialiser (serdes) arrangement, but the lanes can be expanded to six.

"You could ask why not just move to XAUI, which solves the logic and pin out problems of SPI-4.2," said Aruj. One issue is that XAUI is a 10Gbit/s interface, whilst SPI-4.2 supports between 15 and 16Gbit/s. Other differences include SPI-4.2's channelisation, which supports multiple channels over a single physical link, and its flow control enables packet interleaving. "It is all about how you use the bandwidth between two channels [sharing the same interface]," said Aruj.

With SPAUI, Dune has addressed all three differences between SPI-4.2 and XAUI. Moreover, it is making the interface freely available.

To match SPI-4.2's higher throughput, each lane's speed can be increased, as can the number of lanes. To support 16Gbit/s, six lanes at 3.125Gbit/s each or four lanes at 4 or 4.5Gbit/s can be used. "We do both [with SPAUI]," said Aruj, who points out that chip vendors Marvell and Broadcom already use these options with their own XAUI extensions.

SPAUI also adds intelligence in the form of channelisation and flow control. Moreover, SPAUI's default mode supports XAUI. This commonality and familiarity with XAUI is why Dune believes SPAUI is the option of choice for vendors extending 10Gbit/s interfaces. "For vendors, it is not a big jump – they don't have to implement a new asic to interface to us," says Aruj.

This is also Lattice's view and the company is developing a design that interfaces existing devices, such as an NPU that uses SPI-4.2, to SPAUI. Lattice will use its SPI-4.2 IP block and add programmable logic to support SPAUI. "The design will be on the same scale as SPI-4.2 and will require 2000 to 10,000 look up tables, depending on the number of channels used," said Peera.

SPAUI IP development will take two months, but the hardware validation will take longer – between two and three quarters, says Peera. Meanwhile, Lattice is waiting for its customers to give the nod before it begins the SPAUI work in earnest.

Whilst Peera sees SPAUI gaining industry backing, Lattice is not seeing customer requests for the OIF's SPI-S interface. Peera views SPAUI as the simplest and most elegant interface whilst Interlaken, still to be standardised, likely to be the most widely adopted.

Dune's Aruj believes SPAUI and Interlaken are complementary, rather than competitive, interfaces. He believes SPAUI is the best way to implement 10Gbit/s interfaces today, whilst Interlaken will be the next generation interface of choice for designs supporting 40Gbit/s and 100Gbit/s. As for SPI-S: "I don't want to call it dead, but it is," he said.

Dune expects 10 chip vendors to adopt the SPAUI interface. Vitesse has already announced it will use SPAUI for its Barrington-II multiport Ethernet MAC, which will be in volume production in the first half of this year. Besides Lattice and Altera, NPU vendor Bay Microsystems will use SPAUI as the interface in its next generation NPU

"For vendors, it is not a big jump – they don't have to implement a new asic."

Ori Aruj, *Dune Networks*

Aruj claims all leading NPU vendors are committed to SPAUI. Marvell is likely to be an adopter and Dune has a close relationship with the chip firm, which sells Dune's traffic manager and fabric interfaces under its own brand.

Dune expects the first switch equipment using SPAUI to be launched around the middle of 2008 for US shows Interop and NXTcomm.

But don't expect to see 'SPAUI inside' stickers on the new equipment. Only the likes of Aruj, walking around the show floor, will have the quiet satisfaction of knowing the role his company's interface's is playing in powering these latest platforms. ■

Figure 1: 20Gbit/s SPAUI bridging application