

**F**or the past 20 years, the rhetoric of integrated circuit design has been one of increasing exclusivity, despite the falling cost of transistors with each jump in process node. The rise in mask and software tool costs over those same generations has forced many would-be chipmakers to settle for off the shelf microcontrollers and programmable logic.

ARM is one company betting on a reversal in the downward trend of custom IC design starts driven by a surge of interest around applications for the IoT. At the Design Automation Conference, held last month in Austin, the processor designer expanded its programme to attract a wider base of companies to use its low end M-series cores by recruiting tools suppliers Mentor Graphics and Cadence, as well as design houses such as Open-Silicon and Sondrel.

Nandan Nayampally, vice president of marketing and strategy of the CPU group at ARM, said: "The main targets are startups and makers. We are also seeing OEMs in white goods who want to start building their own solutions rather than using standard microcontrollers."

### Filling the capability gap

Chris Shore, training manager for partner enablement, said: "A lot of companies are coming into this who haven't done their own custom SoC before. This programme fills the know-how capability gap that many of these customers have."

Kevin Steptoe, vice president of engineering at design house Sondrel, added: "This class of device turns everything upside-down. The customers are not necessarily chip aware people and they don't have vast sums of money to have a classic EDA tool licensing model."

ARM expects many to use the low-cost prototyping approach known as multiproject wafer – in which masks for a collection of different ICs are put together to be manufactured on the

# Chip design for the rest of us

As the IoT unfolds, classical EDA design flows will need to change. By **Chris Edwards**.

same wafer – to provide samples and even low-volume production parts.

Nayampally pointed to the availability of multiproject wafer services for processes as being relatively affordable, quoting costs of \$16,000 for samples of a 25mm<sup>2</sup> chip built on a 130nm process and \$42,000 for a 16mm<sup>2</sup> die aimed at the 65nm node. Design support company eSilicon slices the wafer even more finely, providing the ability for companies to group together multiple small chips in what would normally be one slot.

Steptoe sees a range of different types of company looking to develop

their own silicon. Among those now looking to build their own IoT silicon will be companies looking to improve the performance of existing designs or to reduce overall production costs or power consumption through integration. Steptoe said: "They've got more than a spec. They've got a design that can be retargeted. I think there will be a lot of those."

More speculative, but on ARM's radar, are companies which have an idea for an IC and, potentially, a system-level model, but which have limited experience in the design process. Because companies coming from those different angles will often have few, if any, SoC designs under their belt, they are likely to turn to design houses to get their ICs to tape out, Steptoe argued.

Mentor Graphics' Tanner EDA group, which has signed up for the ARM programme alongside Cadence, sees its main targets as existing chipmakers that, until now, have left digital integration to others.

Jeff Miller, product strategy and marketing director for the Tanner group, noted: "We have a special package of tools available to DesignStart customers. The idea is that they can buy everything they need to implement a basic SoC and use their analogue know-how for connected sensors for the IoT.

"A lot of people are coming from the analogue side. Now, they want to move into a larger IoT market by adding an MCU, as well as radio IP."

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The companies moving sideways into a market previously dominated by standard microcontrollers are often looking to capitalise on the specialised processes now available for older nodes. “There are people doing high voltage designs that are currently dominated by 180nm BCD processes,” said Miller. “Others are moving to smaller processes because they have substantial digital content, so they are looking at 65nm or 90nm.”

Steptoe said the push to integrate more digital logic into ICs focused on analogue and sensor processing does not change the design flow dramatically; it will still be a matter of synthesising IP written in hardware description languages down to standard cells and then having them organised by a place and route tool. However, the EDA tool suppliers expect customers working on older nodes to be able to benefit from what they have learned implementing designs at the leading edge.

For example, the place and route tool in Tanner’s IoT offering is based on the Nitro engine, which is used for today’s 14nm finFET based ICs. Miller said designs on older nodes can take advantage of the analysis of parasitics introduced to deal with the issues surrounding finFET processes to make it easier to ensure circuits hit their timing targets. “We are

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repackaging it to make it easier to use for the Tanner customer base.”

Synopsys found that when it applied its newer tools to older processes, it was possible to increase overall density because of improvements to placement and routing algorithms. A further advantage, according to Antun Domic, general manager of the Synopsys design group, is that tools developed during the past decade have focused increasingly on power consumption – an issue critical to battery powered sensor nodes. They can more easily cater for multiple power domains on the die that designs were not expected to have when the 90nm or 65nm processes were at their initial peak of development.

Although much of the flow will be automated, Steptoe believes hand tuned layout will be increasingly important element of IoT node design. “Energy harvesting circuitry will require a highly customised approach,” he contended.

The inclusion of MEMS sensors into designs will, however, complicate the flow. Although CMOS based MEMS allows for monolithic integration, a

likely scenario for many projects will be to have two or three devices pulled into a single package.

“Regardless of whether they are packaged or on the same die, they have to be designed together,” Miller argued. “We have a bunch of tools to model the MEMS device, from which we can take the output and feed it as a reduced-order model into the IC design tools to make sure they work together.”

### Analysing trade offs

Tom Beckley, senior vice president of Cadence’s custom IC and PCB group, claimed the need to analyse tradeoffs between board, package and chip-level integration has become more pressing. “Cadence is no longer just focused on EDA. We believe the world of unfolding smart products requires unified solutions.”

The need to build small ICs into flexible boards for wearables and other uses will put more emphasis on the need for codesign, potentially pushing more of the work into the intersection between electrical and mechanical design. The focus may switch from classical EDA flows to those that look at the system as a whole.

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