Mixing it up

Addressing the mixed signal system on chip design challenge.

*By **Rainer Kaese** and **Eugen Pfumfel**.*

No system is ever purely digital and there is a growing requirement for linking core processing functionality with the outside world via analogue and mixed signal IP blocks.

However, a number of factors need to be carefully considered if the inherent – and potentially costly – risks of integrating such blocks into the SoC design are to be avoided.

One of the first decisions in an SoC development will be the choice of process technology. Today's mainstream cmos process offerings cover 130nm, 90nm and 65nm, although more mature technologies remain in production.

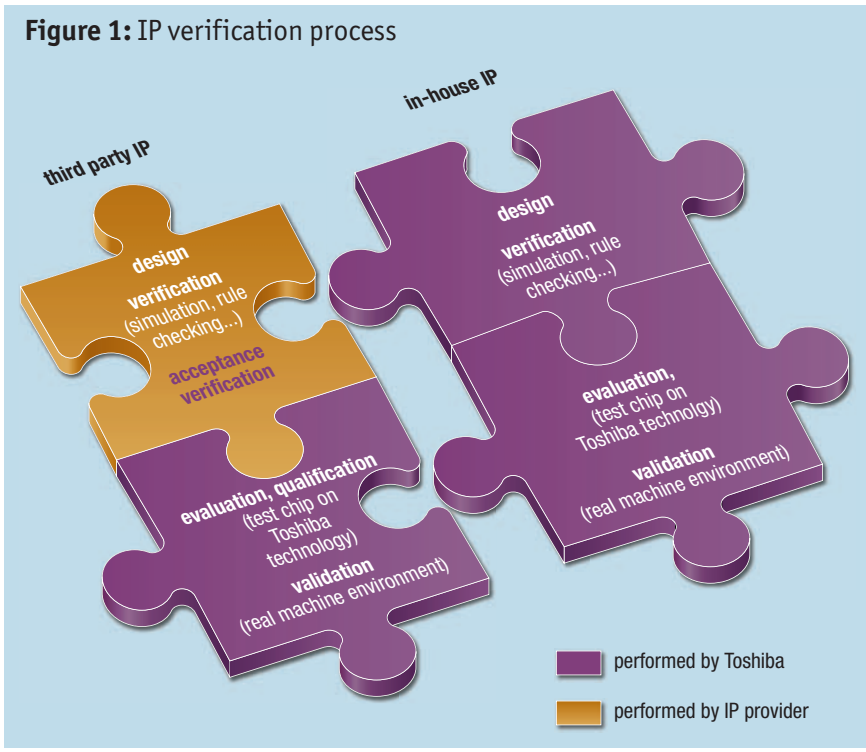
The key is to carefully match the process to the specific requirements of the target application. The performance, size and power demands of next generation consumer and mass market applications may require the high density and low power consumption provided by a 65nm technology. However, an SoC processing a few lines of 2.5Gbit/s PCI Express signal functionality may be better suited to a less costly 90nm process.

At the heart of any SoC solution will be a digital processor; another important design consideration. For instance, licensing ARM technology and the ability to provide synthesisable ARM cores is becoming increasingly important to companies that offer asic development and foundry services.

It must also be recognised that getting the best performance from the digital processor core is tightly coupled with the availability of suitable embedded memories. Each Toshiba asic technology offers a choice of embedded sram, register file and rom architectures; each optimised for a variety of specific applications, such as high density, high speed, low power, efficiency for small blocks, efficiency for large blocks, single port, dual and multiport access. All can be compiled in a range of words and bits.

The requirement to link core digital processing functionality with the real world means that an important consideration is how best to implement the d/a, a/d, serial to parallel and parallel to serial elements.

Figure 1: IP verification process



Rather than designing these elements from the 'ground up', the sourcing of silicon proven, robust analogue and mixed signal and analogue intellectual property (IP) has become critical.

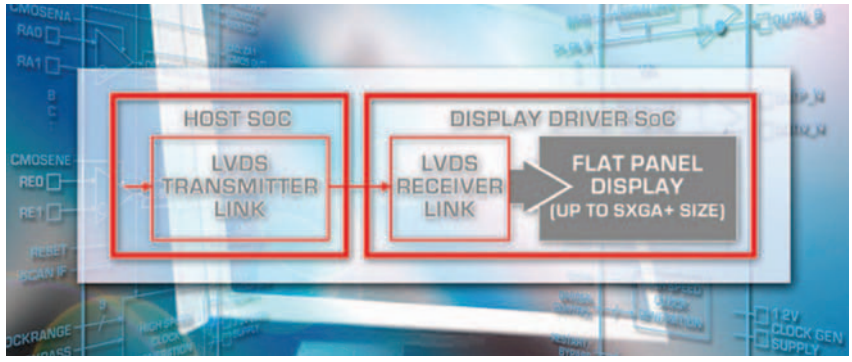
It is this requirement for readily available IP that has led to the emergence of an industry based around third party IP vendors, foundry manufacturing and eda companies. However, a growing number of ODMs, OEMs and fabless chip companies are beginning to realise there are inherent risks associated with this model: in particular, sourcing IP that has yet to be proven in the target silicon.

It is essential, therefore, that SoC designers assess how simple it will actually be to integrate the IP into the target design and how likely it is that everything will work the first time around. Tight time to market windows and budget pressures mean the objective has to be to minimise the technical and commercial risks associated with respins. Among the factors to consider is the potential for the 'blurring' of the boundaries of responsibility – which supplier (IP provider or foundry) will take responsibility for a problem and provide the support needed to resolve issues.

However, IP from independent vendors can prove highly suitable for the rapid integration of standard connectivity blocks into an SoC – at least up to functional sampling. The limitations, however, start to become apparent when it comes to

addressing tough specifications and tight process/production windows. IP for a/d and d/a converters and for PLLs, for example, requires many parameters to be optimised, while the multiple standards and wide range of potential configurations of a serdes implementation means project issues dominate and customisation is almost always needed.

Recognising these limitations means those looking to create advanced SoCs are actively seeking alternative supplier models that can better meet their design and development requirements. One such model is the integrated device manufacturer, IDM. In the IDM model, the supplier provides total SoC competence – from IP development and support to semiconductor fabrication – allowing customers to deal with one organisation from design to manufacture. And an important element of a successful IDM model is the strategy taken towards the ava ilability of mixed signal IP. Toshiba's IP strategy is specifically targeted at minimising risk for the customer.



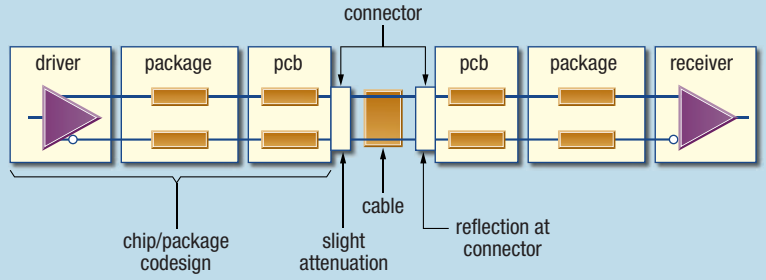
Toshiba's strategy is to provide internally developed and qualified mixed signal IP cores that are silicon proven and optimised for integration into its cmos processes. As an IDM, Toshiba has full access to – and control of – the target semiconductor fabrication process. This means all hard macro IP cores developed in house are guaranteed to be fully compatible with and optimised for the underlying process technologies. In effect, IP design can be optimised and customised with final production in mind from the beginning of the development process.

"The sourcing of … robust analogue and mixed signal and analogue IP has become a critical factor." ***Rainer Kaese*** *and* ***Eugen Pfumfel****, Toshiba Electronics*

However, the strategy also recognises that, in addition to Toshiba's portfolio, customers will still require certain IP from third parties. As a result, whether the IP is developed in house or starts life at a third party design house, it will still be subjected to the same rigorous design verification methodologies. This includes full testing of the IP in target applications as well as validation of the interoperability and system level quality of interface system IP.

A number of customers will want to use their mixed signal IP. In this case, Toshiba can provide a Process Design Kit for the required technology node, as well as evaluation, verification and qualification support to ensure the IP meets the same quality and stability criteria as Toshiba's offerings.

Figure 2: System level signal quality validation



IP categories

Most mixed signal IP can be divided into data conversion (a/d and d/a converters) and connectivity. For the latter category, Toshiba has launched two mixed signal IP cores – the dual link LVDS transmitter (FPD-TX) and the LVDS receiver link (FPD-RX) – designed to simplify and speed integration of LVDS transmitter and receiver functionality into SoC designs for flat panel displays.

Outside of the data conversion and connectivity arena, there are mixed signal IP solutions for phase locked loops and for voltage regulation, in the form of hard macros for LDO regulators. Designers will also find I/O cells to address requirements such as power on reset and non standard I/O voltages.

Implementing advanced SoC designs requires careful consideration of the most relevant processes, the core digital processing technology and the availability of relevant mixed signal IP. For fabless chip designers and OEMs looking to reduce risk and ensure minimum turn around times, there are significant advantages to the IDM business model, where all aspects of the design and development process are handled by one company.

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