

Unifying Microarchitecture for Embedded Media Processing



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As more and more applications require audio, video and communications processing capabilities, the requirements placed on embedded processors used in portable devices and edge-client devices have become more computationally and bandwidth intensive. Both RISC microcontrollers (MCU) and DSPs have served these applications. While RISC processors are traditionally architected to enable efficient asynchronous control flow, DSPs are architected to perform well for synchronous, constant-rate data flow (for example, audio or voice-band applications).

Because so many embedded applications have intense requirements for both control and media processing, engineers have typically turned to inelegantly grafting DSPs and MCUs together in one form or another, either at the board level or in system-on-chip (SoC) integration. Together, the respective functional aspects of RISC processors and DSPs unite as the perfect processing engine for a wide variety of multimedia applications and products, such as cellular telephones, digital cameras, portable networked audio/video devices, and so on. Various MCU makers have incorporated some signal processing functionality, such as instruction-set extensions (e.g., MMX® from Intel, 3dNow!® from AMD, VIS™ Instruction set from Sun, etc.) and MAC units, but even this approach lacks the essential architectural basis required for advanced media processing applications.

It is important to note that engineers are attracted to these kinds of multiprocessor or multicore design techniques for *one reason only*: No single processor has the processing power or instruction characteristics to meet the requirements of their applications. This especially rings true for high performance, media-rich embedded applications. Fundamentally, multiprocessing is only employed in the absence of a viable single-processor alternative. Despite the seemingly simple solution offered by multiprocessing, the reality is that no one would suffer the complexities of a multiprocessing environment except as an absolute necessity to meet the needs of a particular application.

Thus, the need for a powerful “unified” microprocessor for embedded media applications has long been evident. However, it was not until Analog Devices and Intel jointly developed the high performance Micro Signal Architecture (on which all Blackfin® devices are based) that a single architecture was powerful enough, inexpensive enough, and truly optimized both for the complex, real-time world of media data flow and for the control-oriented tasks typically handled by RISC processors. This unified approach to the increasingly media-rich embedded application space is clearly an ideal replacement for previous heterogeneous DSP/MCU integration techniques.

Blackfin takes the unique step of architecturally combining media processing attributes like dual MACs (multiply-accumulate engines, commonly used for high performance DSP applications) and classic RISC characteristics like a memory management capability that facilitates simplified, enterprise-level programming modes and styles. The device has DSP features not found on any RISC microcontroller and important microcontroller characteristics not typically on DSPs. This paper provides an overview of the architectural and functional features that make Blackfin an ideal embedded media processor.

Functional focus

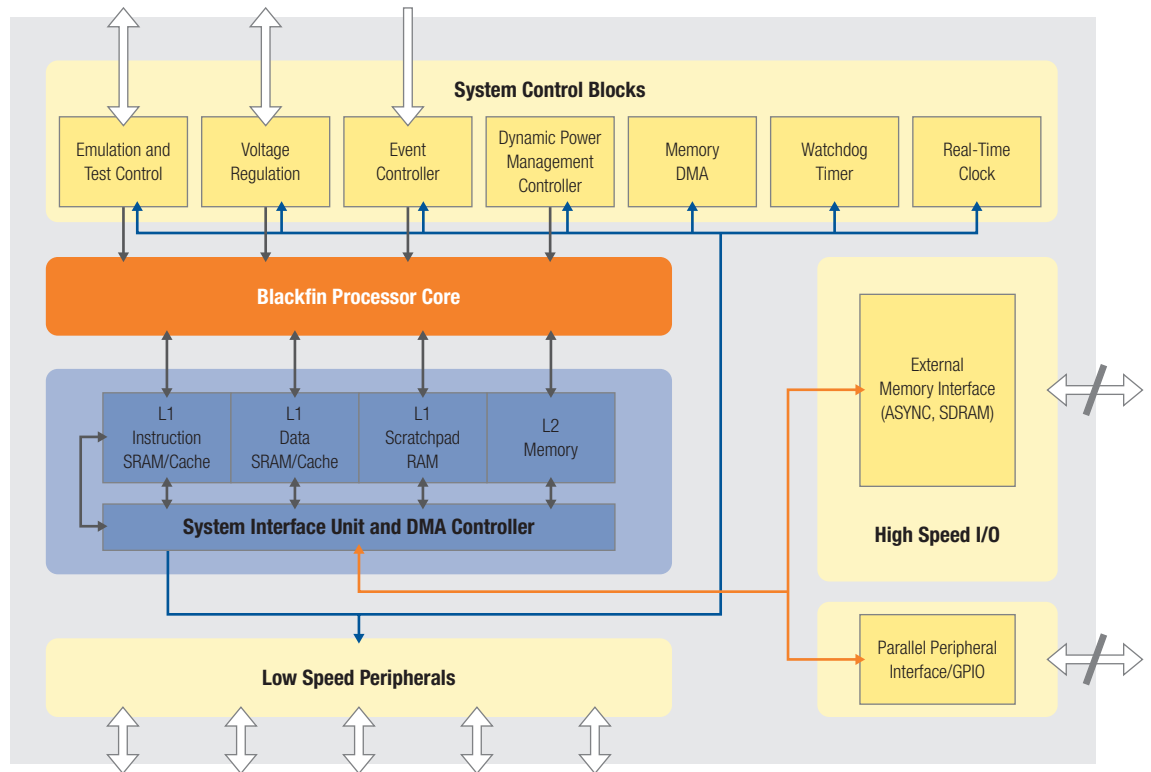
DSPs and microcontrollers have classically remained separate because they are each architecturally optimized for very different kinds of tasks. DSP applications usually focus on performing as many arithmetic computations (such as MAC operations) as possible in the fewest number of core clock cycles. To accomplish this, DSPs often use esoteric VLIW (Very Long Instruction Word) instructions, leaving code density as a secondary concern. Also, DSP applications are data-bandwidth intensive; thus, they often have large memory databuses and DMA engines to reduce the data movement load on the core processor.

For media-processing applications and formats, DSPs require ancillary processors to make up for a lack of flexibility. However, in addition to native support for 8-bit data (the word size common to read red-green-blue pixel-processing algorithms), Blackfin's enhanced video instructions and video ALUs process rich-media bit streams at up to 10 times the performance of DSP-only implementations. The unified architecture is designed to support software that can efficiently execute video compression, motion estimation, and Huffman coding algorithms used by video and image-processing standards such as MPEG2, MPEG4, and JPEG.

Implementing video algorithms in software allows OEMs to adapt to evolving standards and new functional requirements without hardware changes. The core architecture allows for support of algorithms such as MPEG2, MPEG4, and JPEG compression. The integrated video instructions also eliminate complex and confusing communications between the main processor and a separate video CODEC. These features help lower overall system cost while improving the time to market for the end application.

The control functions that are typically the focus of microcontrollers, on the other hand, involve many conditional operations, with frequent changes in program flow. These programs are most often written in C or C++, and code density is vital, making variable-length instructions a crucial architectural feature.

The Blackfin architecture is optimized for both media and microcontroller functions.



The unified Blackfin architecture realizes the benefits of both approaches. Its variable-length instruction set extends all the way up to 64-bit opcodes used in DSP inner loops, but the Blackfin instruction set is optimized so that 16-bit opcodes represent the most frequently used instructions. Thus, compiled Blackfin code density figures are competitive with those of popular microcontrollers, and like virtually all microcontrollers, the Blackfin architecture is optimized for use with a C/C++ compiler. Its fully interlocked pipeline and algebraic-syntax assembly language make it easy for developers to write in either high level language or assembly with equal ease. Thus, Blackfin's architectural nature is not optimized for either media or microcontroller functions at the expense of the other—rather, it is truly optimized for both, and this is the crux of the breakthrough nature of the Blackfin devices.

Enterprise-class features

Because they have system-level responsibilities, true embedded media processors cannot simply operate in the same egocentric fashion as a focused, number-crunching DSP. They must instead have a full set of enterprise-level security characteristics like memory-management capabilities that define separate, freely accessible application-development spaces while keeping distinct code sections safe from being overwritten and the overall system intact. Blackfin, like MCUs that support full-featured embedded operating systems, has both protected and unprotected operating modes. Respectively, Blackfin calls these “User mode” and “Supervisor mode.” These crucial protection features prevent users from unknowingly or maliciously accessing or affecting shared parts of a Blackfin-based system. User mode prevents users or code from doing anything that affects system-level resources. These kinds of security and system integrity issues are simply not needed by nor architected into traditional DSPs.

Like a microcontroller, Blackfin also allows both asynchronous interrupts and synchronous exceptions. Both kinds of events cause pipelined instructions to suspend execution in favor of servicing the triggering event. Blackfin's mappable interrupt priorities are a feature common to microcontrollers, but not usually found in DSPs. The chip's exception-handling capabilities are enterprise-class features that protect a Blackfin-based embedded system from invalid or illegal programming.

In today's security-focused environment, Blackfin's exceptions are an important means of ensuring that no one succeeds in executing an instruction that doesn't exist, or accesses memory that's off limits or not defined (DSPs, on the other hand, allow much easier raw access to the “metal” with few protections). Like other embedded processors, Blackfin can generate interrupts and exceptions in software, facilitating an interface from User mode into the unprotected domain of Supervisor mode.

System-class peripherals with media-class data flow

Blackfin's rich set of on-chip peripherals makes the devices ideal for the control side of embedded applications. Blackfin devices integrate a real-time clock, a watchdog timer, general-purpose timers, bidirectional flag/interrupt pins, SPI-compatible ports and UARTs. Some members of the family include PCI and USB connectivity. These peripherals are typical of control-oriented RISC processors. Blackfin devices also provide streaming-media-oriented peripherals, such as a parallel peripheral interface (PPI) for connecting to high speed video and data converters, and synchronous serial ports for connecting to high resolution digital audio devices and high speed telecom interfaces.

One of the problems many developers encounter when trying to apply MCUs to media-processing applications is supporting memory bandwidth fast enough for streaming data. Embedded media processors unequivocally must have “wide open” DMA capabilities for getting data blocks on and off the chip. With the large amounts of data movement required by most media-processing applications, data movement cannot be permitted to cause processor interrupts that would affect real-time performance, and it is inefficient for the core processor to be

involved in data movement. The DMA channels are independent of the processor core, allowing it to operate deterministically and allowing the DSP data flow in any embedded application to be completely independent of the control processes.

In typical applications, raw data gets DMA'd into the media processor from the chip's peripheral(s), then gets DMA'd to and from external memory during media processing, and then the processed data gets DMA'd back out to the peripheral(s) or to system memory. Blackfin has 16 high speed DMA channels to support bidirectional streaming-media channels between peripherals and memory, virtually eliminating data-movement responsibility from the processor.

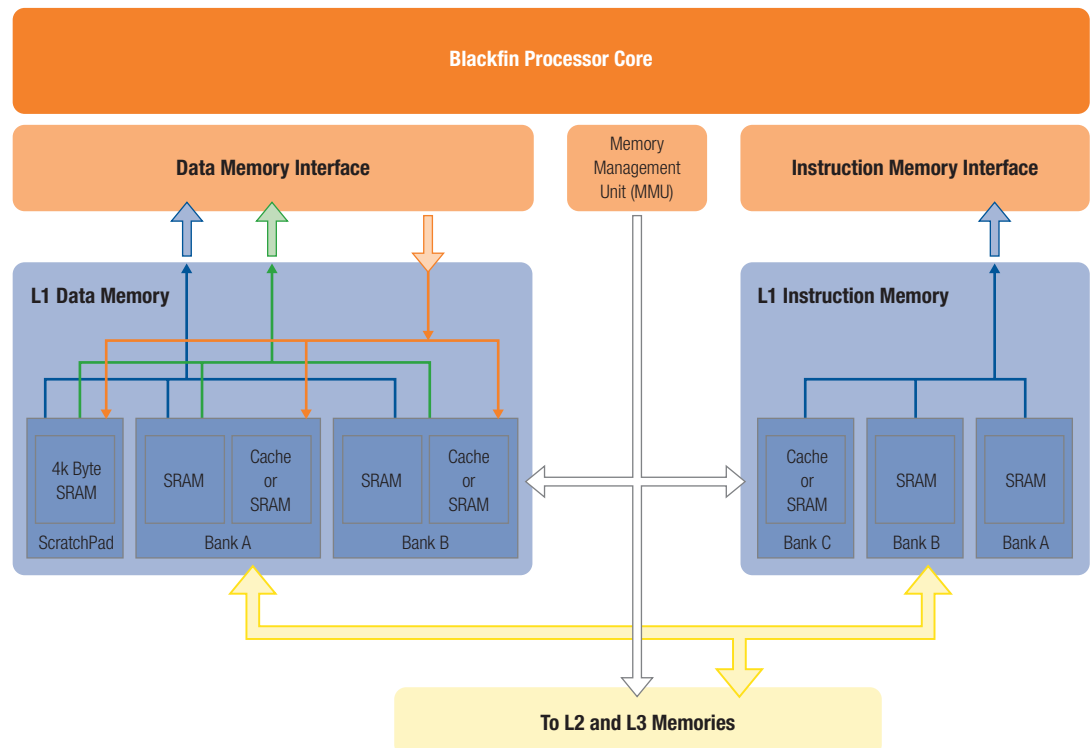
A unified programming model

Blackfin is not a DSP with an enhanced instruction set, nor is it a microcontroller with DSP extensions. The device is an equally high performance media processor and compiler-friendly processor that will be familiar and satisfying to both classes of developers. It allows simple bit-level manipulation, the use of algebraic assembly syntax, and an SRAM memory model for low latency access to assembly modules. Dedicated L1 memory for stack and heap space, dedicated stack and frame pointers, enhanced address generators, and a very large linear address map make Blackfin as good a compiler target as any RISC processor on the market.

The Blackfin architecture allows L1 fast system memory to be defined as either cache or SRAM. This is another example of how Blackfin allows programmers to flexibly tune and trade off performance versus power consumption through the ability to turn on and off unused chip resources. The Blackfin MMU allows developers to protect selected areas of memory and manage system resources (cache and other memory subsystems) in an enterprise-class embedded environment where not everyone has access to all sections of memory and system resources.

Like most microcontrollers, Blackfin has on-chip hardware support for software exceptions, hardware breakpoints, performance counters, and execution trace, plus complete control of the target hardware through a single JTAG port.

Blackfin's memory architecture allows programmers to flexibly tune and trade off performance versus power consumption.



The Blackfin software development model enables high performance DSP functionality within a framework matching that of typical RISC devices. System-level and product-level application code can be written in C/C++ and layered on top of a standard real-time operating system (RTOS). Lower-level code, such as media operations, can be optimized in mixed assembly code and C/C++ code, utilizing hand-tuned, assembly libraries of high performance media functions. Blackfin can be just as easily programmed in assembler, compiled C/C++ code, or a mixture of both.

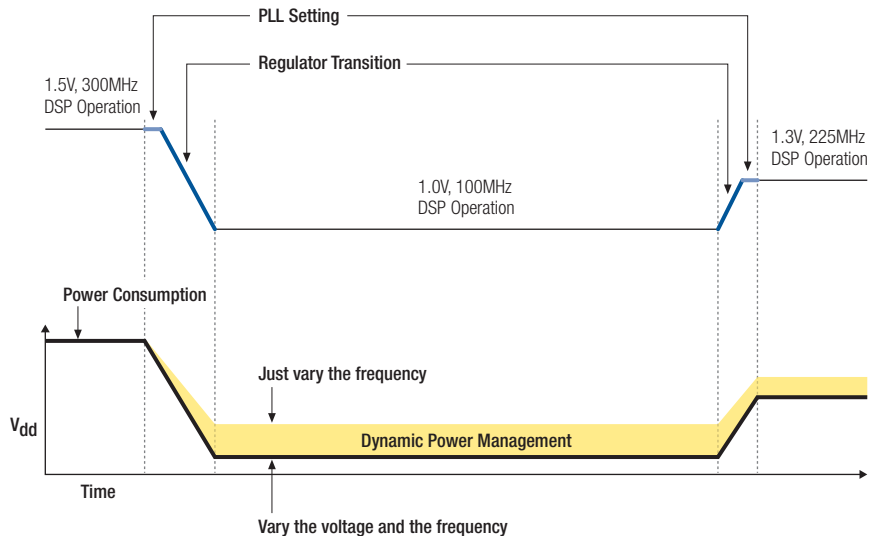
Dynamic power management

Control of power dissipation has long been a major concern for embedded applications that are frequently designed for portable and power-constrained environments. And when embedded systems have needed DSP functionality, choices have been few. When separate MCU and DSP cores are combined on one chip, power control becomes even more difficult and complex.

As an embedded media processor, Blackfin's integrated dynamic power management (DPM) controller can optimally address the needs of a given embedded application. Multiple power modes support a range of system performance levels, and the device is designed to allow selective disabling of clocks to unused peripherals and L2 memory. The PLL frequency can be adjusted over a wide range to save power based on various processing needs, and Blackfin's voltage can be adjusted to enable exponential savings in power consumption.

The fast clock rates needed to meet the computational complexity and performance requirements of an embedded media processor make it difficult to apply tactical power-saving design schemes. Blackfin's dynamic power management capabilities optimize performance versus power for specific tasks, supporting a multitiered approach to power management that adjusts performance based on system needs. Going one step further, Blackfin also allows the core voltage to be changed in concert with frequency changes, so less power is consumed when running a section of code at a lower frequency and a lower voltage, even if execution time is extended.

Blackfin processors optimize power consumption.



Advantages

The advantages of using a single, unified core to replace a separate microcontroller and DSP are many. But the key benefits include reduced cost of ownership and faster time to market. Both these benefits are driven by the ability to use a single tool chain to develop code on a single, unified platform. Instead of having to learn two instruction sets and tool chains, developers can learn one instruction set and maintain a single code base running on a single operating system (where applicable). In fact, because they are architected from the ground up for true embedded media processing, these devices actually define a new domain of “media instruction set computing.” A unified core has one set of software application programming interfaces (APIs) and drivers, one debugger, one loader, one linker, one language, and so forth. A single learning curve means dramatic improvement in development productivity—the savings on debug time alone is enormous.

However, the biggest advantage to using a unified processor that delivers the “best of both worlds” is the applications it can enable at performance and price points previously unattainable.

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