Clocking is critical

Frequency management will play an important role if Ethernet is to be applied successfully in synchronous networks. By ***Roy Rubenstein****.*

The convergence of datacom and telecom networks is placing a number of new challenges on network equipment design.

One aspect of such network evolution is clock synchronisation. Distributing an accurate common clocking signal has long been the basis of telecom standards such as the synchronous optical networking / synchronous digital hierarchy (Sonet/SDH) protocols. Now clock synchronisation is being embraced for Ethernet for backhauling wireless data from 3G cellular basestations.

Maxim's DS310x family of devices aims to lower the cost of clock synchronisation while supporting emerging applications such as a synchronous version of Ethernet.

The timing needs of datacom and telecom equipment are dictated by the networking protocols used by the particular platform. Sonet/SDH uses synchronous clocking. A common, high quality clocking signal is used to ensure the resilient transmission of voice and data traffic. Such clock synchronisation is used for timing on the platform's line cards, between systems at a campus or a central office that hosts the telecom equipment, and even between central offices.

In contrast, datacom standards such as Ethernet and Fibre Channel (for storage) are asynchronous. Here, elastic buffering in the form of fifo memory is used to accommodate timing differences between connected systems. As long as the buffers are sufficient deep, data loss is avoided.

Sonet/SDH is widely deployed in operators' networks and remains part of some operators' next generation platform requests. But the general trend is a shift from Sonet/SDH to Internet Protocol (IP) and carrier Ethernet as the standards of choice for operators' network upgrades. Now clock synchronisation is expanding beyond Sonet/SDH to include Synchronous Ethernet.

To simplify system design while enabling Synchronous Ethernet, Maxim has introduced the DS310x family of clock synchronisation devices.

Maxim's flagship device is the DS3100. "When we entered [with the DS3100], three big mixed signal chips were typically used," said Allan Armstrong, business director of Maxim's communications and timing unit. "The DS3100 replaces all three at a third of the [board] space and cost."

Maxim describes its DS3100 as a timing card on an ic. Two timing cards are used typically in a telecom platform, one as backup. "The timing card is responsible for monitoring recovered clocks from a system's line cards as well as from external timing sources, and selecting the highest quality clock from those sources," said David Baron, product line manager for clock synchronisation at Maxim. The timing card performs such tasks as filtering wander, jitter and phase transients.

The DS3100 takes up to 14 clock inputs from a platform's line cards. The DS3100 monitors for frequency accuracy and clocking activity and can disqualify an input clock should any network impairment degrade the clock signal to a point where it is no longer suitable as the platform's common clock source.

The chip generates output timing signals using digital phase locked loops (DPLLs) and an oven controlled crystal oscillator, followed by a stage of analogue PLLs (APLLs). Both are needed: the DPLL provides long term temperature stability and can synthesize any required frequency, while the APLL provides low jitter. "The combination of frequency flexibility and lowest jitter offers the best of both worlds," said Armstrong.

Also on chip are two T1/E1 transmitters and two receivers as well as framers. "The T1/E1 signals only supply timing information: not [a] data [payload] just phase and frequency," said Baron.

The T1/E1 transceivers interface to the highly accurate timing devices known as building integrated timing supplies (BITS). BITS supplies the common clocking source across systems and even locations. T1/E1 signals are typically used to convey clock frequency and clock quality information for the BITS application.

The DS3100 thus monitors the input clocks from the line cards, and feeds back to the cards a high quality clock. The timing chip also triggers an alarm if an input clock starts to drift, or disqualifies the input clock when it exceeds a hard limit, for example if clock edges are missed or there is other network impairments.

Here the input clock is no longer used and instead the digital PLL generates the output clock using the crystal oscillator and a memory setting. And, via the T1/E1 transceivers, the platform can also transmit and receive the BITS' clocking signals.

Maxim offers two other timing card ic variants. The DS3101, which has no T1/E1 interfaces, is aimed at board designs that use external transceivers; and the DS3102, a lower cost ic that has no T1/E1 interfaces and fewer clock inputs than the DS3100.

Synchronous Ethernet

Sonet/SDH T1/E1 lines have long been used for the backhaul of traffic from cellular basestations. Being a synchronous standard, sharing accurate timing across the cellular network infrastructure has been straightforward. Such stringent timing is needed to avoid calls being dropped as a user passes between cells was not an issue.

Now mobile operators are embracing Ethernet to accommodate the rapid growth in mobile broadband traffic. But replacing T1/E1 lines to benefit from the lower cost and flexible bandwidth increments that Ethernet provides requires a synchronous version of Ethernet. "Getting timing off the network, Ethernet alone doesn't do it with its frequency accuracy of ±100ppm," said Armstrong. "What is needed for cellular is a frequency accuracy of 50 parts per billion."

Maxim's second family of devices – the DS3104 to DS3106 – is designed for use on system line cards. These devices provide timing input to the DS3100 in a telecom platform, for example. The devices also take the line card's clock input from the timing card – for Sonet/SDH, 19.44MHz is used to synthesize the required clock rates for the various ics on a line card, such as the physical layer and framer devices, traffic manager and backplane transceivers.

But the newer Maxim ics serve another important role: for synchronous Ethernet, they support all the clock rates needed – 25, 125 and 156.25MHz.

"Maxim was the first company with a linecard ic supporting Sonet /SDH as well as all synchronous Ethernet clock rates," said Baron. In addition, the DS3104 through DS3106 can synthesize any multiple of 2kHz. This allows a linecard to support both wide area network (WAN) and local area network (LAN) frequencies such as 155.52 and 156.25 MHz, as well as other timing requirements.

The ability to generate frequencies flexibly means that if a new timing requirement emerges, for example to support a new forward error correction scheme, the device is primed to meet it. "Timing requirements such as various forward error correction rates, and clocks required for on board cpus, memories and network processors," said Baron.

The chip also includes a degree of programmability due to an in house designed dsp within the digital PLL. One customer had a particular clock recovery requirement that required a design tweak. By downloading a software patch to the dsp, Maxim could meet the requirement.

Maxim is tight lipped regarding its clock synchronisation roadmap, but it admits that it will have more to say at the turn of the year.

Figure 2: DS3104 block diagram

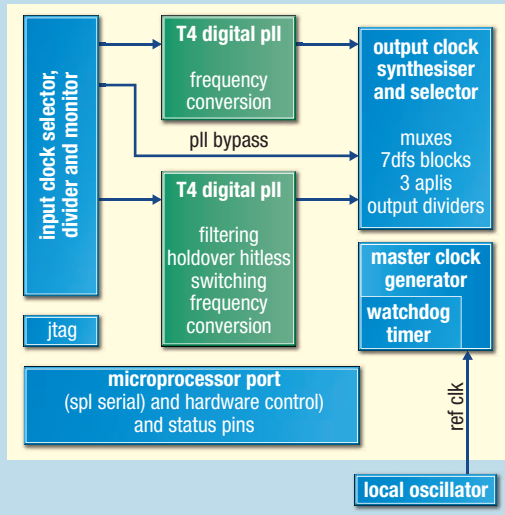

Figure 1: The DS3100 replaces three discrete ics