Electrical Verification of DDR Memory

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Virtually every electronic device uses some form of RAM memory. SDRAM is the dominant memory technology for most types of computers and computer-based products. DDR, or double-data rate SDRAM, has become today's memory technology of choice. It offers a good combination of speed and capacity, power budget, and physical size at relatively low cost-per-bit.

As data transfer speeds increase with each new generation, analogue signal integrity of the memory subsystem has become an increasing area of focus for designers who must guarantee system performance margins, or ensure interoperability of memory and memory control devices within a system. Many performance problems, even ones found at the protocol layer, can be traced back to signal integrity issues. So the importance of doing analogue verification on memory devices is a critical step in validating many electronic designs.

Timing, jitter, and electrical signal-quality tests required to validate memory devices are specified by JEDEC, the Joint Electron Device Engineering Committee. Parameters such as clock jitter, setup and hold timing, signal overshoot, transition voltages etc are included in the JEDEC specifications. But performing tests in conformance with the spec presents many challenges that can be a complex and time-consuming. Having the right tools and techniques can significantly reduce test time and ensure the most accurate results. This article will discuss methods of making memory tests that simplify the validation process.

Signal Access and Probing

One of the first obstacles is accessing and acquiring the necessary signals. JEDEC standards specify that measurements should be made at the BGA ballouts of the memory component. Since FBGA components include an array of solder ball connections that are, inaccessible, how can this be accomplished?

One solution is to include vias on the PCB directly beneath the memory components that can be probed on the back side of the board. Although these test points are not strictly "*at the component ballouts*", signal integrity with this approach is quite good and electrical validation can be performed with acceptable test margins.

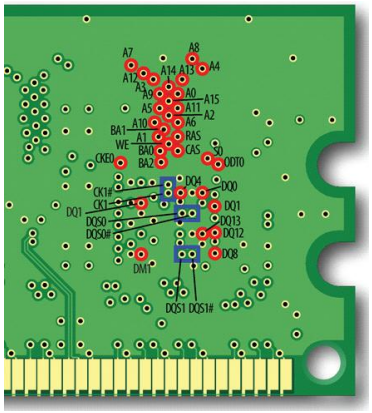

Figure 1: Test points on "back side" vias of DDR3 DIMM.

Although it is possible to use handheld probes for this type of application, maintaining good electrical contact between multiple probe tips and test points simultaneously can be difficult, so the option of using solder-down probe connections is a usually better alternative. Solder-down "micro-coax" probe tips provide a cost-effective solution with excellent signal fidelity and sufficient bandwidth for testing the fastest memory devices up to DDR3 @ 1600 MT/s.

Signal access through back-side vias may not always be an option. Space limitations on the back side opposite the memory components can prevent placement of test points. Many standard DIMMs now have memory components back-to-back on both sides of the board, to increase storage density. How can the test engineer get access to test points in this scenario?

Fortunately, there are now probing solutions for even this situation. "Interposers" are available for standard DDR3 and DDR2 memory devices. These use a socket that solders down onto the target device in place of the memory component. The interposer, which has test points for probing, then snaps into place on the socket and the memory component then attaches to the top.

Small isolation resistors are embedded within the interposer, as close as possible to the BGA pads of the memory component. These resistors are matched to the probe tip electrical network, ensuring excellent signal fidelity. The eye diagram in Figure 2 was made with an interposer mounted on a DDR3-1333 DIMM.

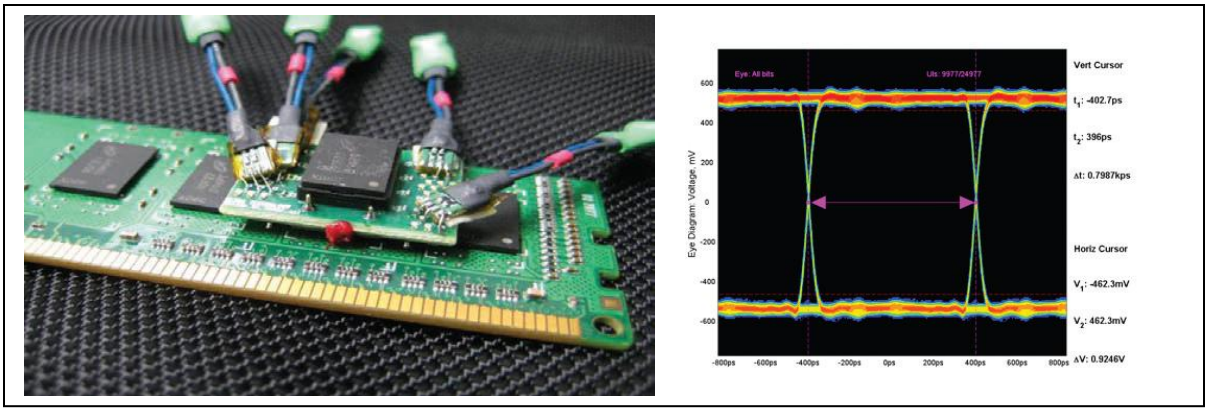

Figure 2: Component Interposer with solder tips; eye diagram of probed signal.

Digital Probing

High performance mixed-signal oscilloscopes (MSO) typically combine four analogue channels with up to sixteen digital channels. The analogue channels can be used to observe clock signals while the digital channels are used to monitor the DDR command bus signals and address lines.

As with the analogue probe, digital probes include a range of solder-in accessories to access difficult test points. Care should be taken to minimize test equipment impact on the measurements. Ferrite cores in the probe tips reduce reflections on the line. Keeping wire length to the minimum required for connectivity will ensure best signal fidelity.

Signal Capture

Once the signal lines have been successfully probed, the next step is to isolate the events of interest on the memory bus. For debug it may be necessary to isolate certain events by a

particular rank or bank, or to isolate specific data patterns for analysis of signal-integrity issues such as data-dependent jitter, timing, or noise problems.

There are several methods that can be used to identify and isolate read- and write bursts or other bus conditions. One of the simplest methods is to use the DQS or Data Strobe signal to identify the start of a read or write burst. For example, DDR3 always asserts DQS high at the start of a write, or low at the start of a read. Hardware triggering capabilities in the oscilloscope can trigger on this preamble portion of the burst and assure that only reads or writes are captured at the beginning of the acquired waveform.

Qualifying Reads & Writes with Advanced Search & Mark

Advanced Search & Mark (ASM) tools, available in Tektronix DPO/DSA70000 and MSO70000 series oscilloscopes, can scan through an entire waveform acquisition and search for a variety of user configurable conditions. One of the conditions available is DDR Read /Write identification; ASM will find all read bursts or write bursts in an acquired waveform record and mark each burst with a visible marker on-screen.

In addition to using these marks for visual analysis, the oscilloscope can apply the marks as qualifiers for DDR-specific measurements, so that measurement occurs only on the appropriate portion of the data stream. In Figure 3, ASM has marked all write bursts with pink triangle symbols shown above the waveform, and a single write burst magnified in the zoom window in Figure 3.

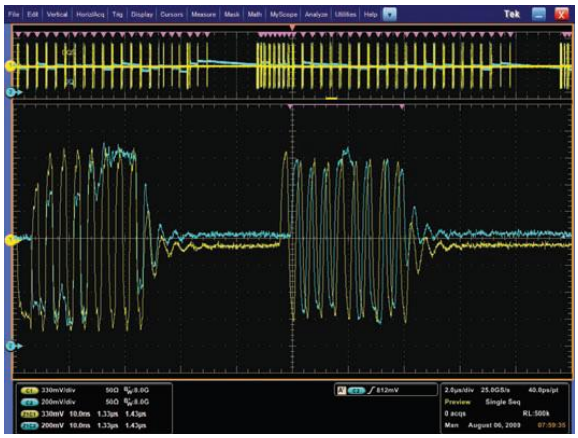

Figure 3: Using Advanced Search & Mark to identify all write bursts.

Bus-Qualified Triggering

The latest mixed-signal oscilloscopes provide many options to qualify signal capture using the state of command and control lines on the memory bus.

SDRAM memory commands are synchronized to the rising edge of the memory clock (CK). The four command signals are chip select (S0# or CS#), row address select (RAS#), column address select (CAS#) and write enable (WE#). The # symbol indicates these are active low signals (see Table 2). The verification of memory commands requires the MSO to probe five signals, CK, S0#, RAS#, CAS# and WE#, in addition to acquiring the appropriate data (DQ) and strobe (DQS) signals. In the MSO digital channel menu the five command signals – CK, S0#, RAS#, CAS# and WE# – are assigned to probe channels.

The Activate Row command is the first command of a write or read command sequence. To trigger the MSO on the Activate Row command, configure the MSO to trigger on a Command group equal to 0011. This is S0#=0, RAS#=0, CAS#=1 and WE#=1, as shown in Table 2. Dealing with binary values like 0011 can be error prone. The MSO works with data in several formats: binary, hex, and symbolic. Pattern symbol files are used when a group of signals define a logical state such as the SDRAM command group.

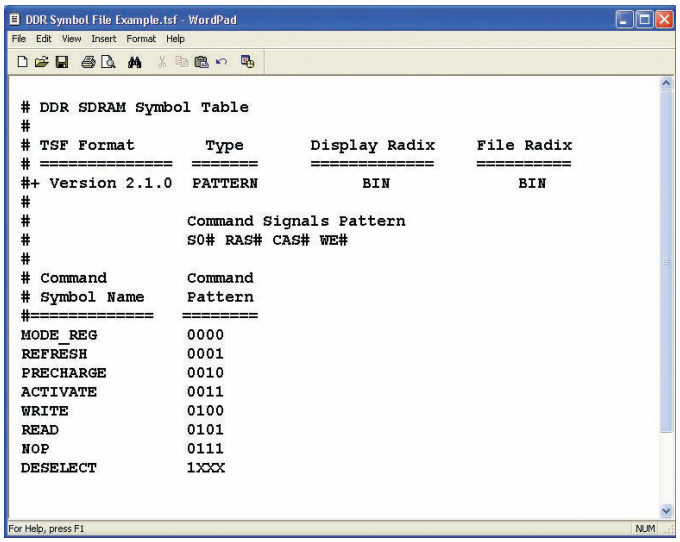

Figure 4: DDR Symbol File Example.

Performing JEDEC – Compliant Measurements

JEDEC specifications for each memory technology include parameters such as clock jitter, setup and hold timing, transition voltages, signal overshoot & undershoot, slew rate and other electrical-quality tests. These specified tests are not only numerous but can also be complex to measure using general-purpose tools.

One example is measurement reference levels; JEDEC specifies certain voltage reference levels that must be used when making timing measurements. Another example is slew rate measurements; Slew rate must be measured on data, strobe, and control signals and is then used to calculate adjustments to the pass/fail limits for timing measurements such as Setup and Hold.

To manage the complex set of JEDEC-specified measurements it can be extremely valuable to have an application-specific measurement utility for DDR test. Using such a utility ensures that measurements are configured properly and eliminates many hours of setup that would be required using general purpose tools alone.

Figure 5: DDR3 Command Bus decoding on MSO70000.

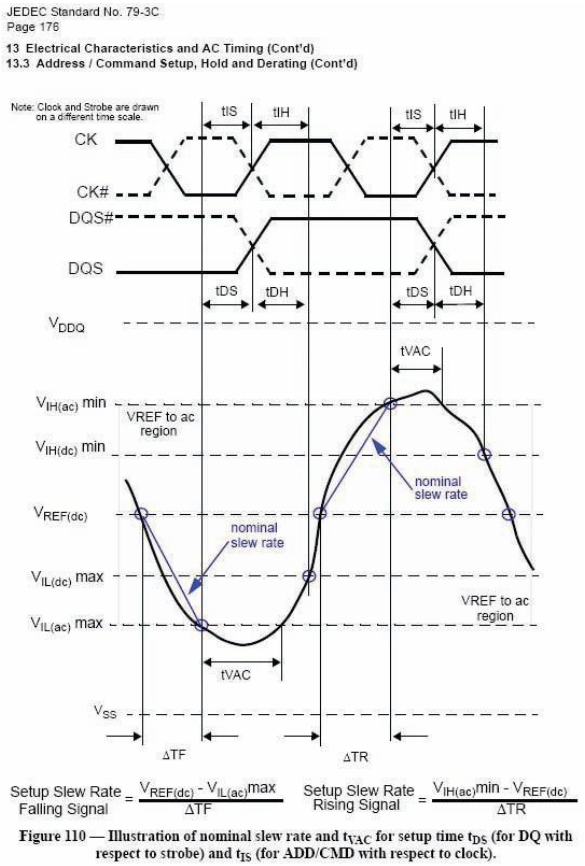

Figure 6: Slew Rate measurement - “Nominal” method for DDR3.

DDR Analysis Software

The broad set of JEDEC measurements by can be automated, such as with Option DDRA on Tektronix 70000 series real-time oscilloscopes.

DDRA works with two other software packages on the Tektronix oscilloscope; ASM (described above), and DPOJET Jitter and Eye Diagram Analysis Tools. These three utilities together create a powerful, flexible yet easy-to-use suite for DDR testing and debug.

The menu interface for DDRA has five steps which guide the user through a selection process. In step one the user selects the DDR generation to be tested (DDR, DDR2, etc) and the speed grade of the memory. Once the generation and data rate have been selected, DDRA automatically configures the proper voltage references for measurements.

Step 2 allows the user to select which measurements to perform. Measurements made on the Clock line are all grouped under a “Clock” drop-down menu. Read measurements, Write measurements and Address/Command measurements are similarly grouped into their own drop-down menus so that all measurements requiring a particular probing setup can be easily selected for a single test run.

The remaining steps 3, 4, and 5 in the DDRA menu guide the user as to how the signals should be probed and offer opportunities for customizing or adjusting parameters such as measurement reference levels. Once the setup is complete and the user selects <Run> the oscilloscope will acquire the signals of interest, identify and mark data bursts, and make the selected measurements. When measuring data bursts, the software automatically generates an eye diagram showing both DQ and DQS overlaid to show relative timing. The DDRA “Results” panel shows all measurement results with their statistical population, spec limits, pass/fail results and other data.

Failure Analysis and Debug

Because all of the captured waveform data is available behind the measurement results, many options are available to the user beyond the results themselves. If a measurement fails the spec limits, it is possible to identify exactly where in the waveform record the failure occurred, then zoom in on the region of interest to investigate the exact signal details and characteristics at the time of failure. Software tools make it easy to analyze the captured data and to pinpoint regions of interest. For example, the Histogram plot shown in Figure 7, can be applied to any measurement of interest, showing worst-case measured values (in this example it has been applied to a Setup measurement.) Several other plot types are available.

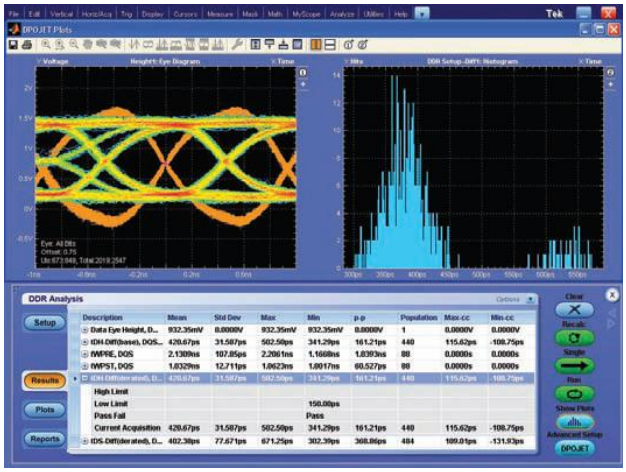

Figure 7: DDRA “Results” Screen showing two of the available plots.

Verifying Command and Protocol Operations

The protocol sequence for a SDRAM Write operation starts with the Activate command followed by one or more Write commands. The Activate command with its row and bank addresses opens a specific row in a specific bank for writes and reads. The Write command with its column and bank addresses opens a specific column in the opened row in a specific bank for writes. It would be a protocol error for the Write command to access a bank that has no open rows. After the Write command, the memory expects at a defined memory cycle that the memory controller hub will write data to it. The row needs to be closed or deactivated with a Precharge command when the writing is completed for the open row and another row is to be accessed. The simplest DDR2 SDRAM command protocol sequence is Activate, Write and Precharge. A consecutive write-to-write sequence is Activate, multiple Writes and Precharge. A write-to-read sequence is Activate, Write, Read, and Precharge. You can have any order of Writes and Reads on an open row. It would be a DDR2 DRAM protocol error if the memory controller hub sent two Write commands in a row without the Deselect command between them. The DDR2 DRAM will respond to the Write command by reading in data that is strobed by the memory controller hub.

In addition to verifying complete read or write cycle operations other important verification tasks that should be performed include:

Basic functional testing
During prototype system initialization a quick check of clock, reset and PLL lines helps to identify any key issues that may propagate into other subsystems. Browser or handheld probes are useful in moving from point to point while checking “vital signs”.

Power management and other special operating modes
As the bus enters and exits power states certain lines may become inactive or turn back on. Careful attention is needed as these additional states add complexity to system interoperability. In Low Power DDR2 (LPDDR2), for example, devices incorporate advanced power management techniques such as Partial Array Self Refresh, allowing only necessary parts of the memory array to be used thus improving its efficiency and power consumption.

Write/Read Levelling
Increasing bandwidth of source synchronous buses can be difficult if only data rate scaling is used. However higher bandwidths can be achieved with innovative physical layer design techniques. DDR3 supports a fly-by topology in which signals from the memory controller arrive at each memory component in a sequential manner, thus reducing loading and improving overall signal integrity. Because of the electrical delays between each component the memory controller needs to perform a delay calibration to realign the clock with the data for each component. Ensuring this operation functions properly helps reduce flight time skews between clock and strobe signals thus providing additional margin to the memory system.

DQ/DQS Margining
As mentioned earlier JEDEC outlines many measurements required for standards conformance. Silicon and component designers are looking beyond evaluation of basic parametric testing to understand and characterize the design over a range of process, voltage and temperature. A common example is to vary the Vref or Vdd lines and monitor data (DQ) and strobe (DQS) for noise immunity and sensitivity.

Combining Digital and Analogue Views

As discussed previously there are many options for accessing DDR signals, from solder-in probe tips to interposers. Many digital lines need to be monitored and then, after uncovering a

signal integrity issue, add another probe to view the signal in its analogue form. This is known as “double probing”, which can compromise the impedance environment of the signals. Using two probes at once will load down the signal, degrading the device’s rise and fall times, amplitude, and noise performance.

With it’s iCapture feature, the MSO70000 allows a user to see time-correlated digital and analogue behaviour, without extra loading capacitance and setup time required for double probing. Any of the sixteen digital channels can be “muxed” through the oscilloscope’s analogue signal path thereby providing a side by side digital and analogue representation of the signal of interest. Figure 9 shows a simple illustration of verifying the Chip Select line on a GDDR5 design. This can be helpful in ensuring correct logic thresholds are used in sampling the digital data or verifying signal integrity with greater precision.

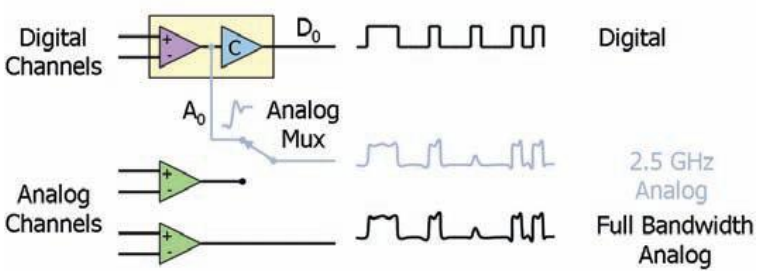

Figure 8: iCapture architecture.

Figure 9: iCapture showing Chip Select line with analogue and digital views.

Summary

In this article we’ve explored many of the challenges associated with DDR testing and have introduced tools needed for validation and debug of memory designs. For more details about DDR testing visit the JEDEC page at http://www.jedec.org/ or http://www.memforum.org/index.asp. Here you will find detailed DDR specifications, white papers, and other support materials. Additional information about DDR testing can be found at www.tektronix.com/memory .