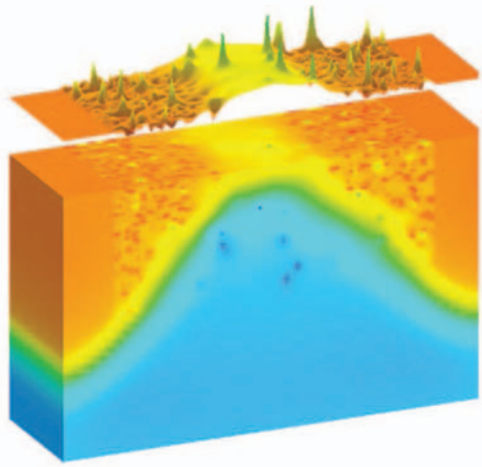
CMOS' future depends on statistics

As semiconductor dimensions decrease, the distribution of dopant atoms becomes a statistical problem. By **Graham Pitcher.**



Random dopants

Nanotechnology evokes images of carbon nanotubes, buckyballs and similar. But Professor Asen Asenov, leader of the Device Modelling Group at the University of Glasgow, has a combative view of what constitutes nanotechnology and how it differs from nanoelectronics. "What the UK considers to be nanotechnology is everything but cmos, but the initiatives are trying to support things that are thought to be electronics. I believe that cmos is true nanoelectronics."

In Prof Asenov's opinion: "This is right in the middle of nanotechnology, where devices have dimensions of less than 100nm."

Prof Asenov believes that nanoelectronics is seen as part of the 'nanotechnology vision' in Europe and he ascribes that to the UK having 'no real semiconductor manufacturing industry'.

Nanotechnology in Europe is being driven, at least in part, by ENIAC, the European Nanotechnology Initiative Advisory Council. ENIAC was set up in 2004 to define common research and innovation priorities to ensure that Europe developed a competitive nanotechnology industry. One of these initiatives is a project called MODERN – Modelling and Design of Reliable process variation aware Nanoelectronic devices, circuits and systems.

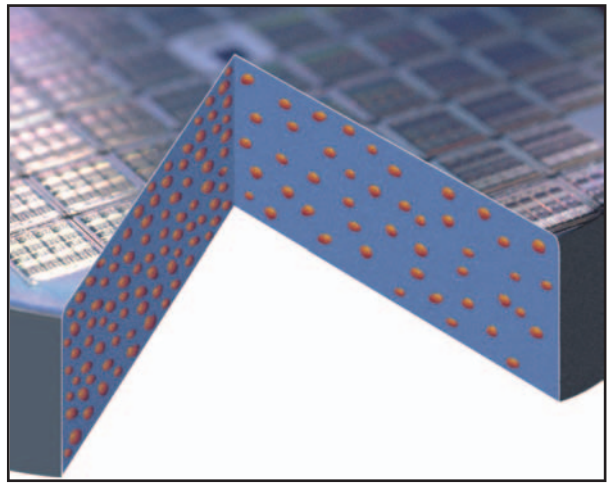
There are fundamental physical reasons for the work, described by Prof Asenov as the 'pudding effect'. "Semiconductors have random dopants and this can be compared to a pudding with raisins. You can cut a piece of this and it may have no raisins; cut another piece and it may have a cluster. Each piece of pudding will be different and that's the same with semiconductors.

"When you get to 22nm and beyond, one transistor may have 10 dopant atoms; another may have 20. That's what causes variability and it's a statistical problem. At the end of the day, that's difficult when a few atoms determine device behaviour."

MODERN has a number of goals, including developing:

- advanced, yet accurate, models of process variations for nanometre devices, circuits and complex architectures.
- effective methods for evaluating the impact of process variations on manufacturability, design reliability and circuit performance.
- design methods and tools to mitigate or tolerate the effects of process variations on those quantities applicable at the device, circuit and architectural levels, and
- validation of the modelling and design methods and tools on a variety of silicon demonstrators.

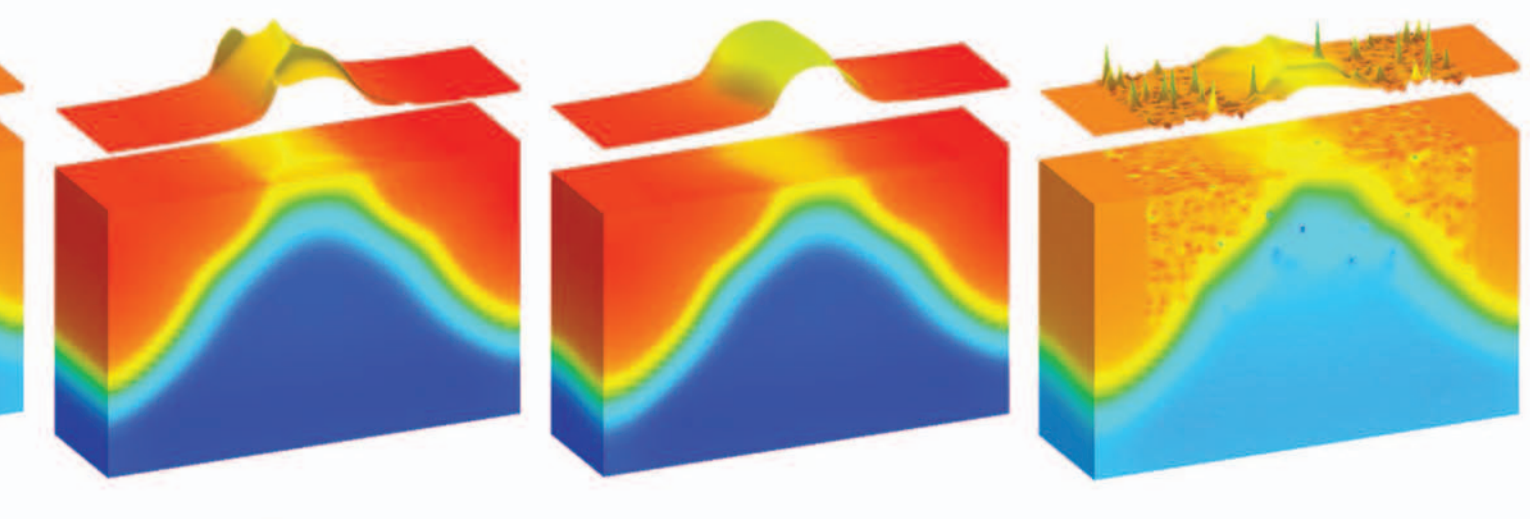
Prof Asenov said: "The project was initially focused on technology itself, but more recently it's not just about making circuits – which is true nanotechnology – it's also about the applications, ranging from infotainment to medical."



Top:
Sources of statistical variability
Above:
Dopant atoms are distributed randomly in semiconductors and, as feature size decreases, fewer dopants will be seen in transistors. Prof Asenov compares this to a slice of raisin pudding: some slices will have more raisins than others and the same will hold with semiconductors

MODERN is about the whole food chain, focusing on advanced nanoelectronic devices, with 45nm considered as the reference."

In essence, however, the focus is well ahead. "We're looking at 22nm," Prof Asenov pointed out, "exploring fundamental problems such as variability." Variability comes in a number of forms: process variability; systematic variability, from lithography and strain effects; and statistical variability, due to the atomic structure of small devices. "Variability is a materials



Poly grains *Line edge roughness* *Combined effects*

issue," he continued, "which can't be controlled by technology."

MODERN is looking to develop a design based solution. "It starts with the simulation of physical variability, capturing these effects in models for use in design. Statistical models can be used in circuit simulation for design verification," said Prof Asenov. "But MODERN also aims to develop counter measures to overcome problems at the design level."

MODERN has a broad focus. "It ranges from device technology to full scale SoC design," Prof Asenov claimed. "It's a complex project with 28 partners, all working at different levels – and the various parts are coming together."

MODERN has a number of layers. "One layer is how you design circuits and consumer products using this technology," he continued. "A second layer is the design methodology and above that are different applications, which are European priorities."

In Prof Asenov's opinion, it is important to link design capability with the overall vision of nanotechnology. "Often, people don't understand that companies such as ARM and CSR are very much part of the nanoelectronics industry because they're designing at the nanoscale."

What he sees is work propagating from the lower levels to inform circuit and system design. "Most of the deliverables from the project's first year were at the lower level. Now, in the second year, we are developing more models. In parallel," Prof Asenov commented, "some partners are looking at different mitigation techniques, including redundancy to compensate for failing components, and ways to monitor what is happening in terms of variability, so voltage or frequency of individual blocks can be changed."

The work is all about extending the life of cmos technology for as long as possible. "CMOS is what we rely on," said Prof Asenov. "Nothing has the potential to take over in the next 20 years."

Driven by Moore's Law, manufacturers push down the technology curve to reduce cost and to increase functionality. "But we pay for this with variability," said Prof Asenov. "So we will have to change the way we think about design to something which is functional from the consumer's point of view, which may fail from time to time, but which should support a stable and reliable product."

Looking further into the future, Glasgow, along with Intel and IMEC, is involved the Terascale Reliable Adaptive Memory Systems project, to determine what might happen beyond the 16nm node. "There is no doubt that Intel will go to 16nm, but it recognises that, while variability problems are large at 22nm, beyond that they become severe," said Prof Asenov.

"At the 16nm node and beyond, a very large number of transistors on a chip will fail or go outside of their operational conditions. But the chip will still have to do what it has been designed for," he concluded.

Ultra thin films may cut threshold voltage

The Ferroelectrics for Nanoelectronics (FERN) project, being led by the University of Newcastle, is investigating the incorporation of ultra thin ferroelectric materials into silicon nanoelectronics.

Ferroelectrics can shrink capacitor size by three orders of magnitude, because of their high electric permittivity. But their capacitance can be made to vary, depending on the applied voltage, which allows very small and tunable capacitors to be made.

Recently, there has been experimental evidence that effective negative capacitance can be seen in ultra thin ferroelectric films. If these films could be incorporated into a transistor, then it would reduce the voltage at which a transistor switches between its on and off states (the sub threshold slope).

The FERN project is looking to make transistors that incorporate the best ferroelectric films to confirm the reduction in sub threshold slope. Ferroelectric capacitors integrated onto silicon will be demonstrated, quantifying the capacitance increase per unit area and examining the fabrication constraints needed to maintain high transistor performance.