Converters cut consumption

Extending battery life and reducing thermal load are two benefits of an a/d converter family. By **Clarence Mayott**

Low power a/d converters are not only needed to maximise battery life in portable applications, but also when devices are housed in small, rugged enclosures where no airflow is possible. Examples include military communication applications, smart antenna systems for WiMAX and LTE, and portable medical equipment: the list is extensive. In situations where the power budget may be capped – for instance, in a femtocell basestation powered via Power over Ethernet – power consumption of each device becomes critical.

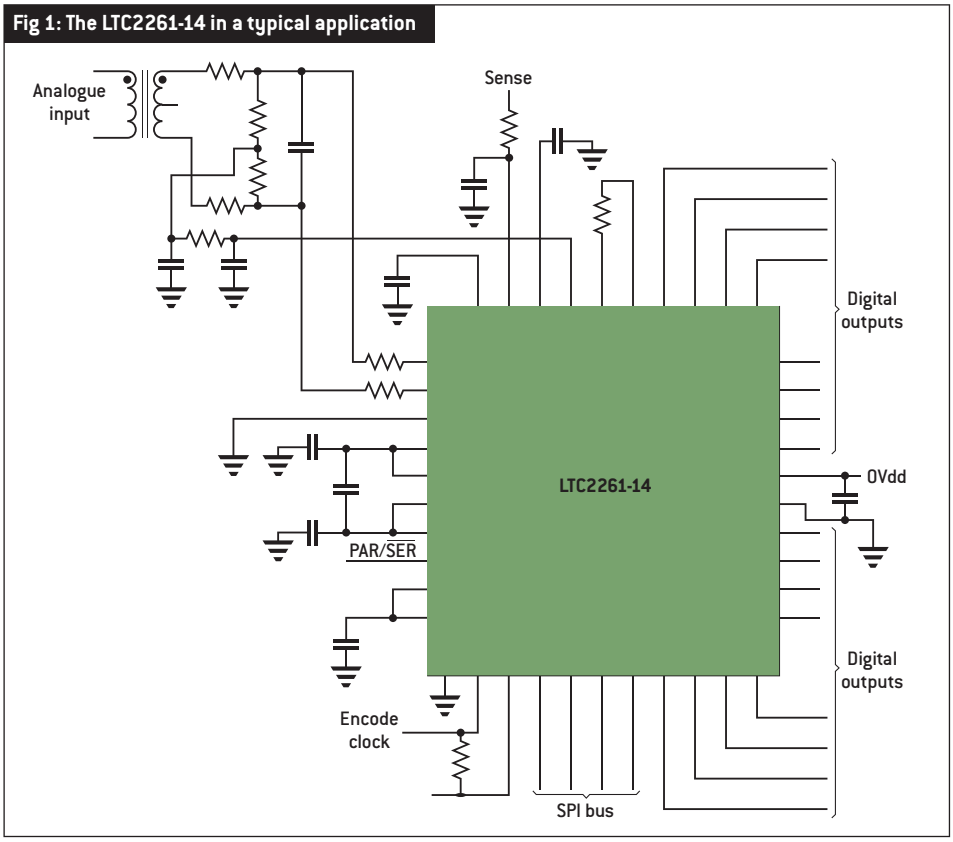
The LTC2262 family of low power, high speed a/d converters dissipates less than one third of the power of comparable earlier generation devices while maintaining excellent ac performance. This makes it possible to improve the performance of power limited applications while remaining within the power budget.

In addition to consuming less power, devices in the LTC2262 family offer a set of digital output features that help to simplify layout and reduce digital feedback. The LTC2262's low power core is also integrated into multichannel parts, including two and four channel a/d converters.

The LTC2262 family includes 12 and 14bit a/d converters that with sampling rates ranging from 25Msample/s (which can sample down to 1Msample/s) to 150Msample/s, while consuming approximately 1mW for every Msample/s. For instance, the LTC2262-14 – a 14bit 150Msample/s part – consumes 149mW from a 1.8V supply.

However, low power dissipation for this pipelined architecture comes without sacrificing performance. The LTC2262-14 has a typical signal to noise ratio (SNR) of 72.8dB and a spurious free dynamic range of 88dB at baseband. Low power operation also improves thermal performance in compact enclosures, where high temperatures can degrade SNR.

Fig 1: The LTC2261-14 in a typical application



The LTC2262 family offers digital features which can simplify overall design. For example, parts can be configured to run in one of three modes: full rate cmos; double data rate (DDR) cmos; and DDR LVDS.

Full rate cmos presents the data on all 14 lines and consumes the lowest power. This mode is identical across Linear's parallel cmos output a/d converters, so designers can use a lower power device without changing fpga code or asic design.

If board space or fpga I/O is limited, the DDR cmos mode can reduce the number of data lines needed. In DDR LVDS mode, two data bits are multiplexed and output on each differential output pair, one valid on the rising edge of the clock, the other on the falling edge. This allows the data to be clocked out on half the lines – seven for 14bit parts and six for 12bit devices.

DDR LVDS mode functions in a similar fashion, with two bits clocked out on each data line on each clock cycle. But, because it is a differential signal, it uses 14 data lines, rather than the 28 lines required for standard LVDS signalling. While DDR LVDS uses an additional 10mW, differential signalling provides some rejection of digital noise, which is also known as digital feedback.

Digital feedback occurs when energy from

converter's outputs couples back into the analogue section, causing interaction that appears as odd shaping in the noise floor and spurs in the output spectrum. This is worst at midscale, where all outputs are changing from 1s to 0s or vice versa, generating large ground currents that couple back into the input.

Digital feedback at the device and system levels can be made worse by poor layout choices. Long output busses, routing at low characteristic impedance and heavy capacitive loading at the receiving device all conspire to produce higher pulse currents in the output stages.

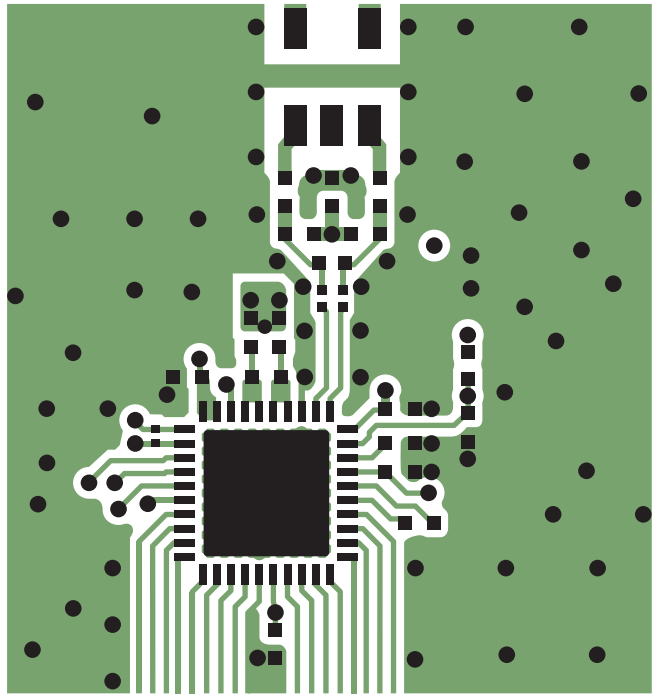
The use of the maximum digital output supply voltage (OVdd) similarly maximises digital currents. Placing the OVdd bypass on the bottom of the board – with added lead inductance, large bodied capacitors, small diameter vias, thick boards and thermal relief – raises the impedance of the supply rails to the output section, increasing the potential for noise sources. Returning digital ground to a poorly grounded paddle makes things worse. Together, these layout conditions conspire to increase ground bounce on the substrate, which leads to digital feedback. This then manifests itself in the converter's output spectrum.

The use of barriers around the analogue input and clock help to reduce digital feedback effects, while proper grounding of the reference bypass and the OVdd bypass help to mitigate digital feedback.

With poor layout and with low signal levels, digital feedback can appear as an exaggeration of odd harmonics. In severe cases, localised regions of the noise floor may be elevated by 20dB. If a narrow band application happens to collide with the elevated region of the noise floor, the SNR can be reduced by 20dB. While good layout can help reduce the effects of digital feedback, it may not eliminate the problem.

The LTC2262 includes a digital feedback mitigation feature called the alternate bit polarity mode. Digital feedback is likely to occur when sampling a small input signal that is exercising a few codes around midscale. On each sample, all high order data bits are swinging from 0 to 1, which generates large ground currents that can couple back into the analogue inputs. When alternate bit polarity mode is used, every odd data line is inverted. So, instead of 14 data lines switching between 0 and 1 simultaneously, half are arranged to switch in the other direction. This produces a cancellation of fields, reducing the resulting ground currents and minimising digital feedback. To decode this data, an inverter is applied to each odd data line in the receiver.

Layout of the LTC2261-14 application shown in Figure 1



An optional data output randomiser is available to further reduce interference from the digital outputs. The least significant bit is combined using an exclusive-OR function with the other outputs before transmission. The received digital output bus can then be decoded by performing the reverse operation in the fpga. Using this data encode scheme reduces the residual tone caused by digital feedback by at least 10dB. Using the output randomiser and alternate bit polarity together can decrease the effects of digital feedback significantly.

The LTC2262 is available in two and four channel variants. The LTC2175-14 is a quad 14bit a/d converter that samples at 125Msample/s and dissipates 558mW – 139.5mW per a/d converter. At 125Msample/s, each channel outputs two bits at a time, using only two lines per converter. This reduces the number of data lines used by the part and allows it to be supplied in a 7 x 8mm qfn package.

The LTC2268 – the dual version of the LTC2262 – dissipates 299mW, or 150mW per converter. It also has LVDS serial output lines that reduce space and is available in a 6 x 6mm qfn package.

Meanwhile, dual and quad versions of the LTC2262 are available in 12 and 14bit formats, with sampling speeds ranging from 25Msample/s to 125Msample/s. Each device shares the LTC2262's ac performance and offers channel to channel isolation of better than 90dB. Serial outputs from the multiple channel parts mitigate the effect of digital feedback, producing a clean output spectrum.

Mayott: "Alternate bit polarity mode ... produces a cancellation of fields, reducing the resulting ground currents and minimising digital feedback."

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