Answering the call

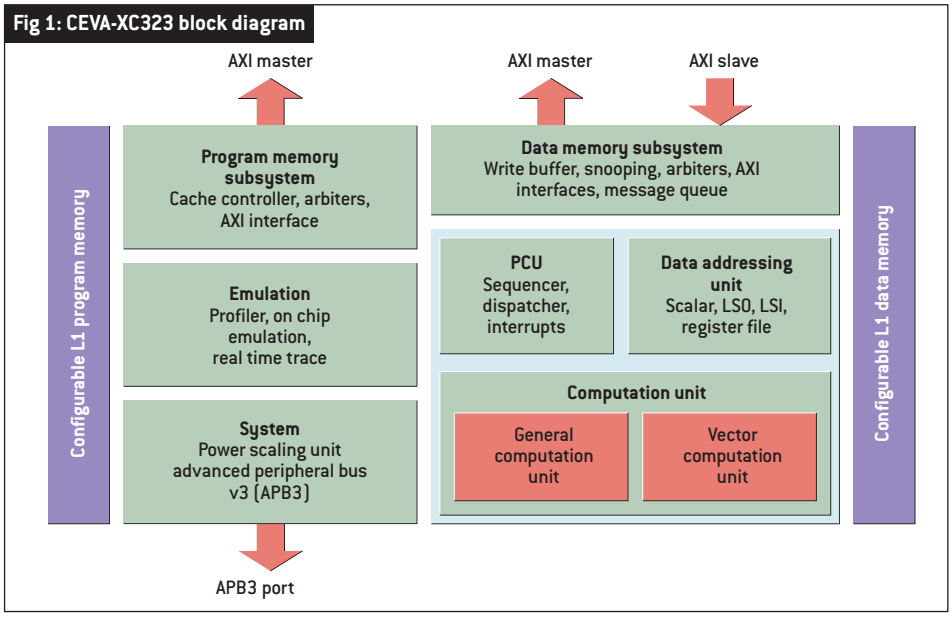
A vector processing core for 4G communications aims to oust discrete dsps from network equipment.
By **Graham Pitcher**

Wireless communications is becoming a complicated business. Although the number of users is not increasing as quickly as it has in the past, the amount of data being 'consumed' per person is booming.

Operators have responded with the development of higher data capacity services, such as HSPA+ and LTE, but this has brought further problems. Eyal Bergman, director of product marketing with IP licensing specialist CEVA, explained. "The move to higher bandwidth with HSPA+ and LTE means more and more data is being carried over the network and this is causing a bottleneck in the infrastructure."

A further complication is the rapid rate at which smartphones, such as the iPhone, are being adopted. "When the iPhone was introduced," Bergman continued, "every network saw the quality of service (QoS) degrade and this has continued as new services are introduced."

Fig 1: CEVA-XC323 block diagram



Part of the problem is the way in which the mobile phone network has been designed: large cells have been created and these serve many users. As there is only so much bandwidth per cell, QoS suffers. "Operators aren't able to extend these cells as much as they want because of regulations," Bergman believed, "so they need to improve their QoS."

A further complication is the business model employed by many operators; one which sees little revenue from data. "While operators need to invest in new equipment, the revenue stream is only growing slowly," said Bergman. "This means they can't justify big investments and this affects the way in which next generation networks will be deployed."

Meanwhile, with energy costs rising, operators are realising that efficient use of electricity has become a critical factor in basestation design.

One way in which operators have attempted to deal with the data problem is by offloading traffic from the mobile phone network on to the existing wired network. A range of equipment has been developed to help in this regard; femtocells are the latest addition. "This is opening up a big market," Bergman believes. "There will be large volumes and it is forecast that 40million femtocells will ship in 2014; many of these subsidised by the network operators."

But the OEMs building network equipment

face equally difficult choices. As the mobile phone has moved from generation to generation, the amount of technology and its level of sophistication has increased. According to CEVA, while the PHY in a 2G communications voice network could be enabled using an asic or an fpga, 3G networks needed large fpgas and multicore dsps, while 4G will need what Bergman described as 'very large fpgas and arrays of standard multicore dsps'. "4G will become very expensive," he noted.

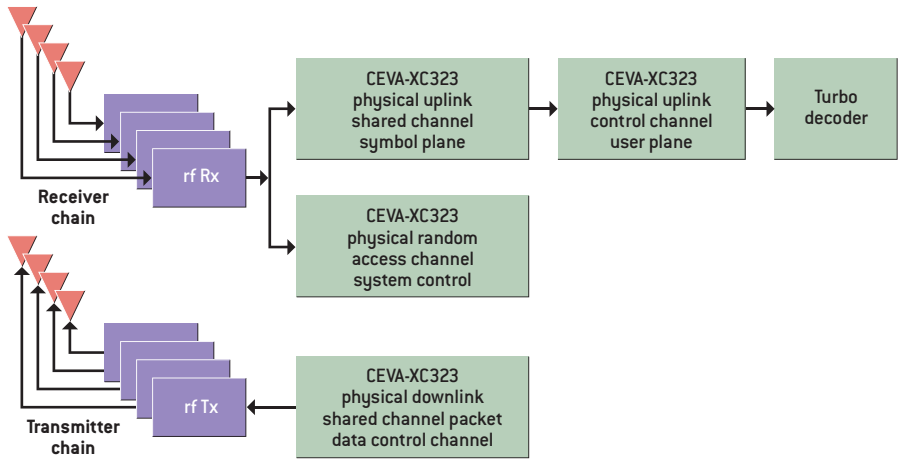
However, another approach is being promoted, based on converged multimode SoCs. These devices feature vector processors, providing multimode support mainly through software. The devices are scalable, allowing the same architecture to be used in a range of products, and integrate the PHY and the MAC with upper layers. Above all, says CEVA, these SoCs are cost effective, allowing equipment builders to move away from dsps and fpgas. "More can be done in software," Bergman contended, "allowing the amount of hardware to be reduced."

This move to a software based approach is being taken, in part, because OEMs have a large amount of software to apply. "One of the big issues is software investment," Bergman continued. "OEMs have huge amounts of software which they want to reuse and to be able to continue to use in the future."

Looking to address these issues, CEVA has launched the CEVA-XC323, a high performance vector dsp for 4G wireless infrastructure applications. The device is said by its developer to deliver up to four times the performance of the dsps currently used in network applications, while lowering the bill of materials through what is said to be a 'significant reduction' in the number of processors and hardware accelerators required.

The CEVA-XC323 integrates two high precision vector communication units designed specifically to cope with the heavy processing load found in basestations. It also supports the homogenous multicore designs commonly used in modern infrastructure architectures. In addition, the core incorporates support for wireless infrastructure control plane processing, which CEVA says is typically handled by separate processors. When complemented with CEVA-XCnet software partners, the core is said to offer a full 3G/4G PHY solution, shortening the development time of multimode wireless infrastructure designs.

Fig 2: A CEVA-XC323 based single sector LTE macro cell



"It's the first vector processor designed for infrastructure applications," Bergman said. "It's scalable and includes the elements needed for hardware acceleration, as well as providing a migration path."

The CEVA-XC323 core combines conventional dsp capabilities with advanced vector processing units to offer higher instruction level parallelism, including: eight way vliw, 512bit SIMD operations, 32 MAC operations per cycle and native support for complex arithmetic. CEVA-XC323 also supports non vectorised operations, control plane functions and system code. It also provides instruction set support covering the most time critical PHY transceiver parts, including MIMO detectors, interleaver/deinterleaver and support for Viterbi decoding in software.

In Bergman's opinion, vector processing is becoming more popular. "Instead of processing, say, 32bits of information at a time, the vector processing units in the CEVA-XC323 can process up to 256bits. And, because there are two such units, the device can process up to 512bits at once. This is bringing higher performance because the devices are working on vector data; instead of processing small elements, they can process large amounts of data."

The device includes an integrated power scaling unit, which provides advanced power management for both dynamic and leakage power. The core supports multiple voltage domains associated with the main functional units – such as the dsp logic, the instruction and data memories, and so forth – and supports multiple operational modes, ranging from full operation to complete power shut off.

Bergman also noted that new features had been added to the dsp core in order to allow it to be integrated into the multicore SoCs now being developed for wireless infrastructure applications. Included are: wide AXI buses for large data transfers; message queues, for synchronisation and system control; and atomic access to external memories. "There is also a snooping mechanism," Bergman continued.

Code compatibility has been an important design parameter. "Software investment is an important issue for OEMs," Bergman asserted, "and our challenge is to allow them to migrate from one platform to another. The CEVA-XC323 is compatible with the code used with Texas Instruments' C6x dsps, so users can take that code and run it on the CEVA dsp 'as is'."

The CEVA-XC323 is scalable from femtocells to macrocells and is said to provide benefits when used in any of these applications. "A typical basestation (macrocell) supports three sectors," Bergman pointed out. "A three sector LTE Cat 5 macrocell running at 20MHz and with a 4x4 MIMO would need 36 dsp cores, plus supporting hardware. An SoC based approach would require only 9 or 12 CEVA-XC323 cores."

Bergman said the core was already being designed into products and he expects announcements to be made early in 2011. "And we have a good backlog of potential orders, which should bring additional design wins in the next quarter."