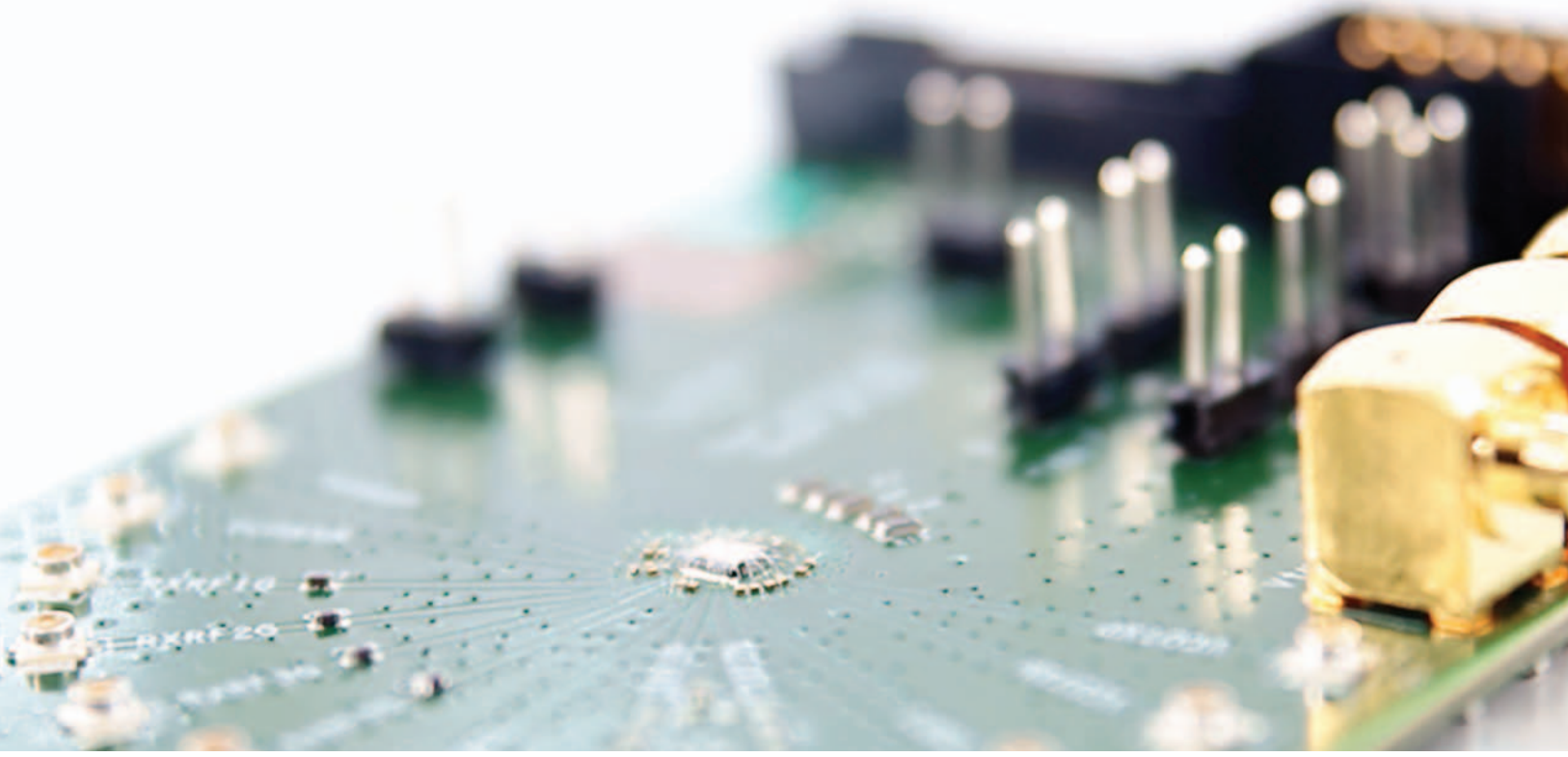


Digital takeover

Analogue designers are having to be increasingly innovative to overcome process scaling problems. By **Chris Edwards**.

Analogue integrated circuit design has never been easy. But as fabs start ramping their 28nm processes, the problems facing designers trying to put mixed signal circuitry on to the chips have reached a new level of complexity.

According to Professor Franco Maloberti of the University of Pavia, process scaling into the deep submicron region brings one crucial improvement: speed. The unity gain current frequency is almost inversely proportional to the square of the gate length, so sub 45nm processes push cmos into the realm of 60GHz wireless communications.

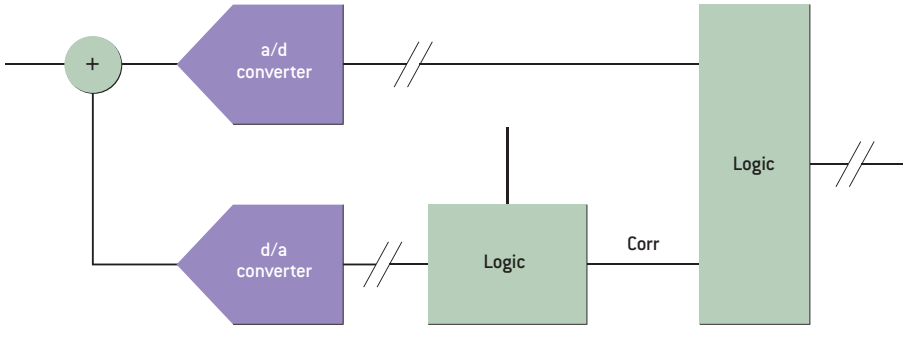
Bert Gyselinckx, programme director at IMEC's Holst Centre, says a good reason for moving the researchers' rf architecture to a 40nm process was 'a matter of having the speed of the technology'. "We use it both for 2.4GHz and 3 to 10GHz ultra wideband radios. That is a challenge for a 0.13μm process."

Unfortunately, just about everything else that matters for analogue circuitry gets worse.

The biggest problem lies in transistor gain. Shorter transistor channels lead to smaller transconductance values, largely because the speed of electrons or holes moving hits a peak before the electric field used to open the channel reaches its maximum. This, in turn, puts a limit on the current that can pass through the transistor: a factor that process designers have been fighting with a combination of strain and increased doping levels.

Dimitri Antoniadis of the Massachusetts Institute of Technology says strained silicon has allowed a 'remarkable increase in velocity that

Fig 1: Background calibration of an a/d converter with added analogue test signal



has allowed scaling to continue'. "But we can't go much above where we are today. There is no more room for carrier-velocity improvement."

A further problem is that analogue circuitry has to fit a digital way of working. Traditionally, mixed signal processes have come with well characterised simulation models, largely because many wafers have been processed, diced and measured over the years. Digital designers working with processes that may not ship in volume until their project is finished have learned to live with models that are inaccurate or change frequently as the foundry's engineers run increasing numbers of test wafers. Analogue designers aiming to put circuits onto these chips have to live with equally inaccurate models and design circuits that can resist the inevitable shift in transistor parameters.

Although Wolfson Microelectronics works on what are now considered mature processes – typically 0.18μm – it has found ways to deal with some of these problems, having decided, for cost reasons, to implement its mixed signal devices on fab lines originally designed to handle digital processes.

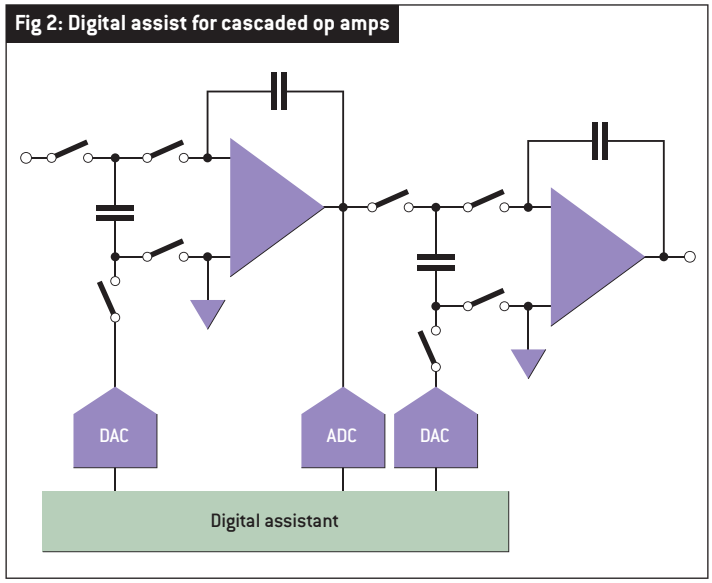
"The sweet spot continues to be 0.18μm and will serve us well for the near to medium future, while 0.13μm can be adopted without a significant amount of redesign. Beyond that, it's a strategic decision; it will come down to how much dsp technology you want to add in," says Nick Roche, director of global applications.

At the same time, Wolfson has used circuit design techniques to overcome the low voltage headroom of even 10 year old processes such as 0.18μm or 0.13μm. One example is a charge pump designed for a headphone amplifier to allow high voltage swings within the circuit and make it possible to remove an external coupling capacitor from the pcb. "And you can make it multilevel for Class G amplifier designs," claims Roche.

To reduce power, the charge pump has a variable frequency clock. This reduces switching losses when the pump can work at a lower frequency.

Others are now looking to older processes for mixed signal work as they face problems trying to combine massive amounts of digital logic with analogue on deep submicron processes.

Fig 2: Digital assist for cascaded op amps



The risk of falling behind in integration is leading instead to a repartitioning of some products, such as the baseband processors for mobile phones. Traditionally, voice codecs and I/O ports were built into this part. But, according to Roche, this circuitry is moving out of the baseband so it can become even more digitally focused.

"Baseband suppliers were desperate to offload voice so they could put their digital baseband devices on deep submicron processes," says Roche. "It was an opportunity to bring voice into the fold: using an i^{2}s or pcm connection across the pcb. So now we are doing voice and audio conversion."

Even though some functions are moving off chip, there are still good reasons for putting analogue onto deep submicron chips. One is simple economics; if you can make it work, a single chip is often cheaper, unless the analogue circuitry – which rarely gets smaller on its own – works out to be a significant portion of the die. Another is that some functions have to stay on chip; phase locked loops have become necessary elements in SoCs. Then there are power and temperature circuits, used to make sure the SoC works correctly. And, with the trend towards software defined radio, more rf focused analogue is turning up on SoCs.

Liesbet van der Perre, director of IMEC's green radios programme, referring to IMEC's Scaldio radio platform, argues: "When people say analogue doesn't scale, we say look at Scaldio over the last three generations."

Design elements have to change, says van der Perre. "We have been building with fewer passives, because passives don't scale well. And you have access to new a/d converters that exploit the speed of the technology."

With high bandwidth a/d converters, it become possible to build radios that can 'sniff' the airwaves for other users and, in principle, use protocols that use gaps in the radio spectrum to send messages. "We can go up to 6GHz in this current version," van der Perre claims.

To try to keep analogue circuits on-chip as processes scale, engineers have come up with a variety of techniques. One option is to combat the loss of transconductance by improving voltage gain. You can use cascodes with local feedback to increase output resistance. However, cascodes can be problematic when there is not much voltage headroom – particularly problematic when the supply voltage is now hovering around 1V – because it's not possible to stack transistors in a classic cascode arrangement.

Mismatch becomes a big problem with low-voltage processes. Techniques to deal with this include chopper stabilisation and auto-zeroing, using a capacitor – which can end up quite large and expensive to implement – to store an offset for cancellation. An alternative that becomes increasingly cost-effective in deep submicron processes is to simply use more digital logic to store calibration and offset values.

The idea of using digital calibration can be taken further. For example, it's possible not just to provide an offset value digitally, a signal processor might use tests on an A/D converter to linearise it's output. Alternatively, a network of small A/D and D/A converters might be used to bias op amps to keep them in their linear operating region, a technique described by Maloberti and colleagues at the summer Circuits and Systems conference in Paris.

As the economics of scaling swing further in favour of logic, digital technology will eat further into the heartland of analogue circuit design.