Converting opportunities

Data converters set to help meet comms systems challenges. By **Graham Pitcher**.

As the number of mobile phone subscribers continues to climb, pressure is growing on the communications infrastructure to support the amount of data that is expected to be downloaded in the future.

In fact, it is predicted that there will be 7billion subscriptions by 2015 – more than one for each of the Earth's inhabitants. And many of these will be using mobile broadband, a trend being reflected in the 25% per year growth in such usage.

Matthias Feulner, Texas Instruments' EMEA marketing manager for telecoms, said: "All of this is having a major impact of telecom systems. Along with demand for higher data rates, users also want more bandwidth and this means new data converters are needed."

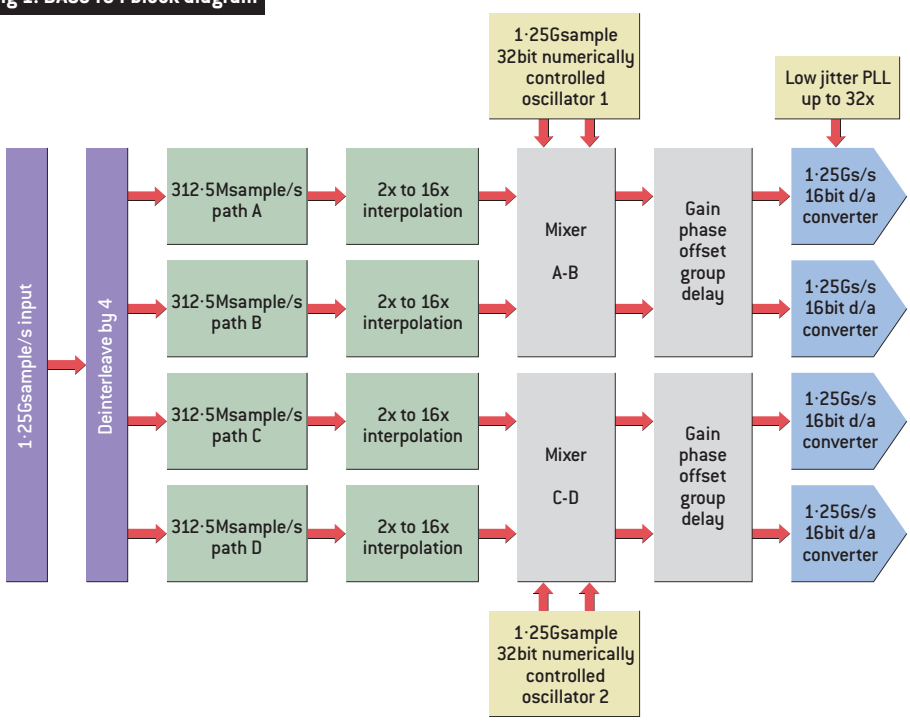
But data rates and bandwidth are only two aspects of the problem facing data converter developers; users are also interested in reducing power consumption and reducing board level complexity.

Texas Instruments has recently unveiled a potential solution to these challenges in the shape of the DAC34xx range of d/a converters. According to Feulner, the parts are 25% faster than the nearest competitor, consume 65% less power and are smaller. "This means developers can create denser systems which consume less power; and this is good for those addressing communications applications."

Over the years, TI's d/a converter portfolio has expanded, with higher sample rates and better resolution. But the DAC34xx range represents the leading edge, with sample rates of up to 1.25Gsample/s and 16bit resolution. Previously, the leading edge was represented by the single channel DAC5681Z and the dual channel DAC5682Z, which supported sampling rates of around 1Gsample/s at 16bit resolution.

TI has accomplished this by developing what it says is an 'all new' d/a converter core. Hans-Peter Beckemeyer, director of analogue marketing, EMEA, for TI, said: "The core takes advantage of low power, high speed cmos, in combination with novel design techniques for power savings and speed improvements."

Fig 1: DAC3484 block diagram



Despite the attractions of other technologies, the DAC34xx range is cmos based. Beckemeyer said: "CMOS offers small transistors at an affordable cost and small transistors translate into two things: more density for large digital blocks; and the lower parasitic capacitance required for speed. CMOS processes also typically allow for lower power consumption."

An example of how much performance has been generated by the new core can be seen by comparing the DAC34xx range with the DAC568x family. Beckemeyer noted: "At 1Gsample/s and with 8x interpolation, the DAC5682Z consumes 1350mW, or 675mW/channel. Under the same conditions, the DAC3484 consumes 850mW, or 212.5mW/channel. That's almost 70% less power per channel."

The DAC34xx range uses current steering, which supports the high resolution as well as providing rapid settling times. Beckemeyer pointed out that current steering in d/a converters is a proven architecture. "It dates back more than 15 years, providing improvements in speed, performance and density. The output current (if current sourcing) or input current (if current sinking) is set by the use of a full scale current setting resistor external to the converter. Each d/a converter has two outputs and the sum of the

current from the two output pins is always equal to the full scale current. Assume, for example, that it's set at 30mA. At mid scale code, each pin has half the current, or 15mA. At full scale digital code, all of the current (30mA) is 'steered' to one output pin, while the other will have none."

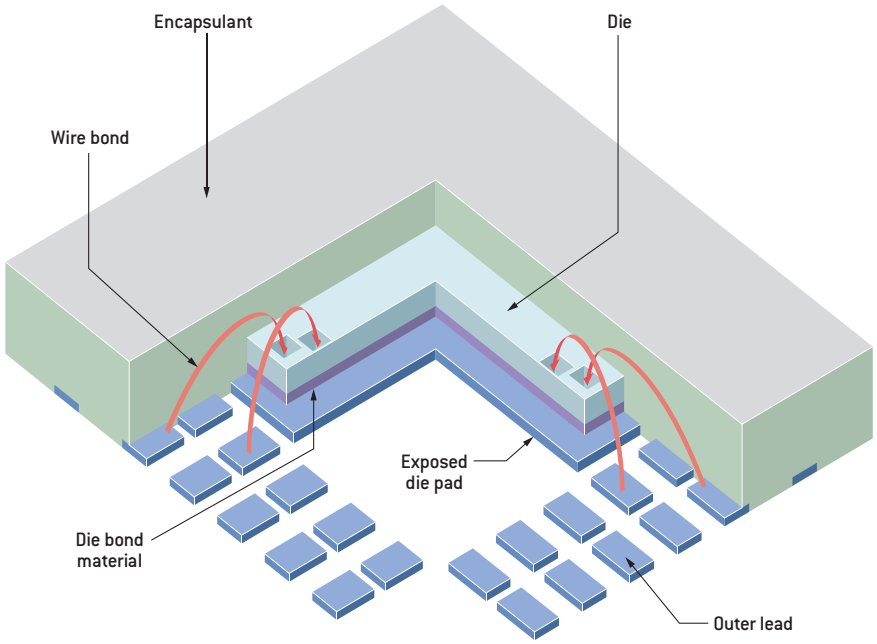
While the DAC3484 and its two fellow parts have been designed primarily for use in the communications world, there are applications in the industrial and defence markets, amongst others. Beckemeyer noted: "These devices were designed with the wireless infrastructure market in mind and, based on the significant interest we've seen from our basestation customers, we expect the lion's share of our sales to be in that market, followed by defence and industrial. We expect sales to be about 80% communications, 10% defence electronics and about 10% industrial, mainly test and measurement.

"In the industrial market, the DAC3484 allows wider frequency ranges with one single measurement, which reduces test time for automated test equipment and signal and waveform generators. Additionally, in radar applications or software defined radios, these converters can help customers to implement very wide band transmitters, reducing scan time during radar scans and increasing the frequency agility of software defined radios."

Applications are also envisaged in the medical sector, where devices such as electrocardiograms, ct scanners and infusion pumps may benefit from the resolution and sampling rates.

The three parts in the DAC34xx range accept a 1.25Gsample/s input. This input signal is then de interleaved by two or four, depending upon which device is used. The resulting two or four data streams then pass along independent paths. Feulner said: "Fewer input channels means there will be fewer input capacitors and that will reduce board design complexity. This is particularly important in multichip systems."

Fig 2: The DAC3484 comes in a multirow qfn package



The devices also feature a block of two or four interpolators, programmable to x2, x4, x8 and x16. "Interpolation is useful if the application doesn't require high data speed," Feulner claimed. "By running at a slower rate, interfacing with fpgas and asics becomes less complex."

These precede one or two mixers, which work alongside 1.25G 32bit numerically controlled oscillators (nco). "Designers looking to implement multichip systems, to support beam forming, for example," Feulner added, "need to include tight synchronisation. We've made sure this can be done easily by integrating two 32bit ncos on chip to create an intermediate frequency. And both ncos can be adjusted independently."

A further block allows gain, phase and offset to be adjusted between channels. "It's important," Feulner believed, "because if there is offset between channels going into quadrature, that affects the system's level of performance. So it must be possible to compensate for these differences."

Gain, phase and offset correction also allows for carrier feed through to be eliminated and unwanted sidebands to be reduced. "If you then apply group delay calibration," he continued, "you can suppress the unwanted sidebands to the noise floor."

The final block in the device is the d/a conversion itself, which can be driven by an independent clock. This can be external to the part or stepped up from an internal clock using an x32 low jitter pll.

TI has also designed the part with digital predistortion in mind. "To do that," Feulner continued, "we have to be able to measure non linear products up to the fifth order. So, if you need 40MHz, you have to sample to 200MHz to capture them. Similarly, if you need 100MHz, then you have to sample to 500MHz at the power amp's output. That's where devices such as the DAC3484 come in."

Three devices are currently announced. Alongside the DAC3484 are the four channel DAC34H84, which has a wider input bus, or the two channel DAC3482. In order to meet board space requirements, two of the devices – the DAC3482 and 3484 – are being supplied in a multirow qfn (see fig 2). The DAC34H84 comes in a 12 x 12mm 196ball bga.

Feulner: "Fewer input channels means fewer input capacitors and that will reduce board level design complexity."