Meeting analogue ambitions

How mixed signal asics can meet cost and performance targets.
By **Shimon Raviv** and **Bert Monna**.

Custom analogue/mixed signal asics are economical at comparatively low volumes, with affordable non recoverable engineering (NRE) costs, meaning a custom chip design can be considered more readily than previously.

Demand for high performance, feature rich analogue end products are driving ever more ambitious requirements for analogue and mixed signal (AMS) circuitry. However, AMS design is notoriously a 'black art' that requires an almost innate ability to trade off multiple parameters simultaneously and to optimise for many unpredictable factors.

Increasingly, the required performance cannot be met using standard components; parts meeting all requirements in terms of functionality, signal integrity and power consumption for groundbreaking new designs are often not available. Some functions can only be achieved satisfactorily in a monolithic asic.

Successful custom mixed signal projects must be supported by accurate analogue models, which display consistent and repeatable parameters. Transistor threshold voltage (V_t) is critical to analogue design; a low V_t enables stacking of transistors, while avoiding the need for high voltage control signals. On other hand, an excessively low V_t can result in high leakage current and greater power consumption. Demands for large resistor and capacitor values also have a strong influence on the optimal process node.

Experience of analogue asic design is central to good decision making. The insights of experienced chip designers are critical; depending on the functions available at various nodes, a smaller overall die size may be achieved using a larger process geometry.

A single chip custom design can help to overcome some technical challenges and mitigate design risks. Integrating the required functionality on one die can eliminate many variables and allow system behaviour to be predicted more accurately.

Making the right decisions

While lower development costs allow a custom chip to be considered for more system designs, the investment remains considerable and sound technical and commercial decisions must be made at the correct points.

The choice of process node is a key factor that can determine whether the functional, performance and cost requirements will be met. Unlike a purely digital design, finer process geometries may not deliver significant performance or cost benefits. Although meeting technical requirements is critical, cost factors, such as tooling and die size, must also be considered.

In the wider sense, identifying the most suitable foundry can determine the success of the project. A number of factors must be considered, such as the level of support required. Meanwhile, high production volumes may be beyond the capacity of smaller foundries, while larger foundries may not provide the attention needed by smaller projects.

The project team must be sure the foundry can satisfy any relevant independent approvals. EquipIC took into account minimum stipulations laid down by the smart card industry, for example, when selecting a foundry as part of a recent chip project.

EquipIC and SystematIC worked on a project that required an output driver capable of operating at up to 18V. Since a 130nm process cannot support this, node selection was restricted to larger geometries, such as 180nm or 350nm. Although the required performance could be achieved at either node, the higher cost of tooling at 180nm drove the decision to choose 350nm. EquipIC and its technical partners also generated the chip specification for this project and developed a 4.5kV ESD structure for I/O pads to enable the chip to perform reliably in hazardous environments.

Libraries and methodology

One of the most important aspects is the quality of the foundry's libraries. Good process characterisation – such as accurate ESD and

Raviv: "A custom chip can be produced for around half the cost of five years ago."

Spice corner models – is critical for successful analogue chip design. However, library accuracy can vary between foundries and is often difficult to predict; experience has shown differences of up to 20dB in the performance of analogue functions between that predicted in the design manual prediction and seen in prototype silicon.

Assessing the available IP is also important. Although basic analogue IP is offered by most foundries, effective IP arguably does not exist for high performance designs. At the leading edge, requirements are individual and call for true custom design to meet area, power consumption and bandwidth requirements. Reuse is usually confined to knowledge, rather than functional blocks.

While it is more difficult to ensure production units are 'right first time' than in the past, advanced toolsets and methodologies make this feasible. However, tools are not a substitute for an experienced design house's knowledge.

Design Rule Checking, for example, provides a valuable detailed verification of the design and its implementation using the selected foundry's process; it will protect against errors in implementation, but creating an outstanding product remains the designer's responsibility.

Arguably, it is more important to follow a proven methodology, calling in the right tools at the right times to verify the design at critical stages (see fig 1).

From concept to asic

During the design process, the target package and test solutions must be considered, determined by customer preference, cost and technical specifications or requirements.

Package design has a significant impact on asic performance, especially for high frequency transceivers and rf products. Both package and asic need to be simulated together.

Proper test is vital before the chip can be released for production and the test methodology must be in mind during the design phase. Selecting the appropriate tester (or test platform) and the appropriate analogue test house partner are crucial.

EquipIC recommends developing test programs in partnership with a professional test house close to the design team. This approach is usually faster and more cost effective, particularly in the early stages of the project. After test time and yields stabilise, it can be economical to port the test programs to the foundry and the packaging house for mass production.

Cost considerations

Although custom chip can be produced for around half the cost of five years ago, most expenses are incurred in development; production cost may be 10% of that of a comparable non custom solution. While an asic project typically begins to deliver returns at a lower production volume – owing to the reduced overall cost – the minimum number of units remains a critical yardstick.

Against this backdrop, asic design teams face tougher engineering challenges. Systems houses are pushing for the best possible performance, demanding not only increased functionality, but also higher output drive capabilities, lower quiescent current, greater accuracy and wider bandwidth. Meeting these targets demands judicious compromises to ensure optimal performance.

Over the last decade, system complexity has increased significantly, while the time available to complete the project is much shorter. As system complexity increases, designers must analyse many more interactions between design elements and the implications for process assembly and test. Meeting project milestones brings intense pressure to deliver 'first pass yield' samples of first silicon to the customer. Determining when the design is ready to go to tapeout is a finely judged decision. Bringing an AMS project to a successful conclusion demands careful attention to detail and judicious technical and commercial decisions, while taking advantage of experience gained from throughout the asic supply chain.

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Fig 1: A typical custom asic design trajectory