Know your limits

As high speed interfaces at the board level push towards 10Gbit/s, signal integrity issues need to be addressed properly. By **Patrick Carrier**.

The ever increasing bus speeds in modern electronics means engineers are now required to have a thorough understanding of issues associated with high speed design.

With serdes bus speeds approaching 10Gbit/s and becoming commonplace in many designs – as well as wider, parallel buses, such as DDR3/4, entering the GHz realm – it is more important than ever that signal integrity issues are addressed properly. Analysing these buses – including comprehensive loss modelling of traces, assessment of via performance using 3d modelling and the inclusion of system timing – is vital to meeting time to market and ensuring design success.

Larger ic packages, along with the increased speed of signal edge rates, make it impossible to measure signals in a typical lab environment; the signal at the die will look nothing like the signal at the pin. As such, it has become even more crucial to rely on comprehensive signal integrity simulation to provide an accurate characterisation of system margins. For serdes buses operating in the multiGHZ realm, such as PCI Express and Serial ATA, this means the inclusion of all loss factors and impedance changes.

Most of the losses in pcb designs can be ascribed to copper and dielectrics. Copper losses include the skin effect, which increases with frequency and becomes more severe around 5GHz when the surface roughness of the copper starts to exacerbate the issue. But dielectric loss is normally the dominant factor and is determined by the dielectric material used in the stackup. The best way to minimise these losses is to use shorter traces, but using wider traces and lower loss dielectrics will also help.

Signal degradation can also be caused by impedance discontinuities, the most notable of which can be caused by vias. Vias can be designed to match the trace impedance for differential signals, but a good via solver will be needed for this. Also, at higher gigahertz frequencies, a 3d field solver should be used to capture the appropriate electrical characteristics of the via structures. In addition to having a different 'characteristic impedance', vias can also have stubs which severely degrade their performance at higher frequencies. Figure 1 shows an example of a 10Gbit/s serdes channel simulation using a 3d via model to solve for the effect of via stubs. Such simulations can be used to identify the need for certain design changes such as the use of blind vias or backdrilling.

Vias are often characterised by a 3d field solver as scattering, or S-parameters – frequency domain models of the vias. Other components of a serdes channel, such as connectors and cables, can also be characterised using S-parameters and this approach can be used to describe the entire interconnect, including connectors, vias and

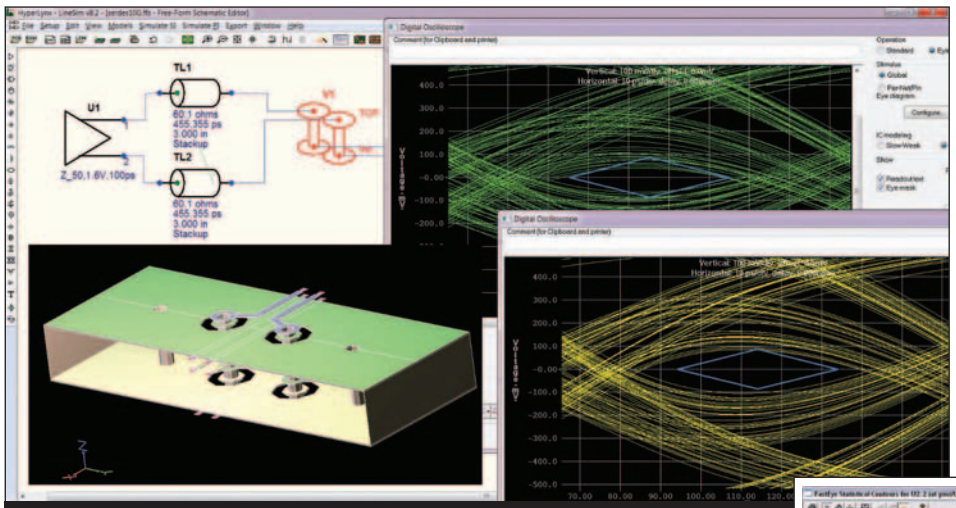

Fig 1: Simulation of a 10Gbit/s serdes channel in HyperLynx using 3d via models

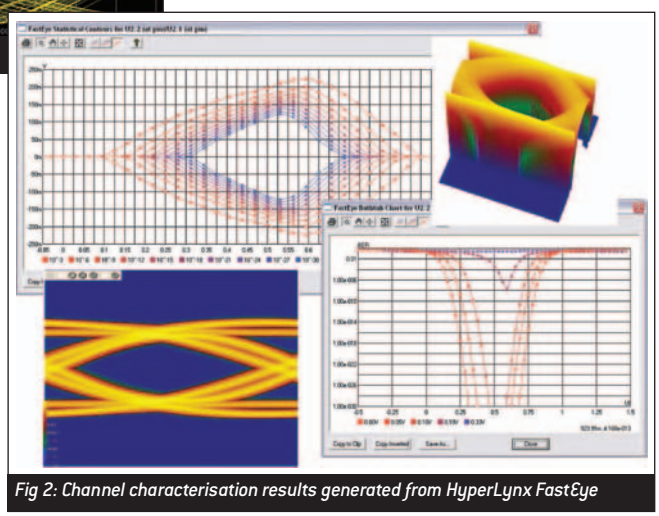

Fig 2: Channel characterisation results generated from HyperLynx FastEye

traces, and then compared against a predetermined loss budget to determine the bandwidth of the interconnect itself, without including the driver and receiver.

In all cases, it is important for a simulator to be able to handle these S-parameter robustly. S-parameters should be able to be converted to allow for appropriate concatenation, enforcement of passivity and causality and, most importantly, to be simulated in the time domain. Even though the interconnect can be analysed as an S-parameter, doing so does not allow for inclusion of the effects of pre-emphasis and equalisation, which are crucial to many faster serdes channels.

The inclusion of signal conditioning techniques such as pre-emphasis and equalisation is yet another reason why simulation is being relied upon to characterise serdes channels, as it is impossible to measure this in a normal lab set up. The need for signal conditioning has also spawned indirectly a number of developments in the analysis of serdes channels. This includes the use of 'channel analysis' or other fast eye diagram creation techniques, as well as new modelling standards such as IBIS-AMI. Because of the complexity of serdes drivers and receivers introduced by these signal conditioning techniques, typical I/O buffer modelling methods, such as IBIS models, are insufficient. As such, many designers have fallen back to using SPICE models for this task. Unfortunately, SPICE models are far too detailed to allow for practical system level simulation or the very long simulations needed to characterise channels to bit error rates (BERs) of 10^{-12} or 10^{-15}. However, SPICE models can be used in conjunction with channel analysis techniques, such as Mentor's FastEye, to verify channels to these BERs in a reasonable amount of time.

Channel analysis techniques, such as FastEye (see fig 2), use pulse and step responses to characterise an entire serdes channel, including the driver and receiver, and to build eye diagrams and bathtub curves based upon those responses. This allows for these channels to be characterised to very low BERs and for the effects of all deterministic and random jitter to be taken into account. That just

Carrier: "It is more important than ever that signal integrity issues are addressed properly."

isn't possible when performing a bit by bit simulation with a SPICE model.

This type of analysis is also the basis for an emerging serdes modelling standard called IBIS-AMI. IBIS-AMI models contain an analogue buffer model, which is used for generating the step response of the channel, as well as a compiled .dll for modelling the pre emphasis and equalisation. A comprehensive serdes simulation not only includes an accurate and complete model of the interconnect, but also models the complete driver and receiver behaviour to the target BER.

But it is not only serdes buses that have driven advancements in signal simulation; other buses are also pushing the boundaries of system margins and DDR3 is an excellent example.

DDR3 (and DDR2) goes beyond the typical VIL and VIH voltage threshold method for determining timing – VIL is the maximum voltage recognised as a logic low, while VIH is the minimum voltage for a logic high – to use an approach called slew rate derating. Here, a series of tables based on edge rate is used to determine more accurately when the input gate will actually switch – something which is crucial to the system timing. DDR3 also includes write levelling, which is a per byte deskew necessitated by the daisy chain architecture of the address bus routing.

These complicated timing relationships can be difficult to analyse. Having a simulation tool, such as the DDRx Wizard in HyperLynx, can allow an entire bus to be simulated at once and for the complicated timing relationships in the bus to be reduced to a set of simple pass/fail criteria.

Fast single ended buses like DDR3 (see fig 3) also generate other issues which can be difficult to analyse. While via modelling is important for these buses, a more important aspect is to understand how the vias are bypassed and how they interact with the power distribution network. Other power integrity issues, such as voltage drop and ensuring adequate decoupling capacitors, are come to the forefront because of the high speeds, high currents and low operating voltages used by these buses.

Having a comprehensive suite of simulation tools to address these issues will be essential in the future for anyone undertaking high speed pcb design.

Author profile:

Patrick Carrier is a technical marketing engineer for Mentor Graphics' high speed pcb analysis tools (**www.mentor.com**).

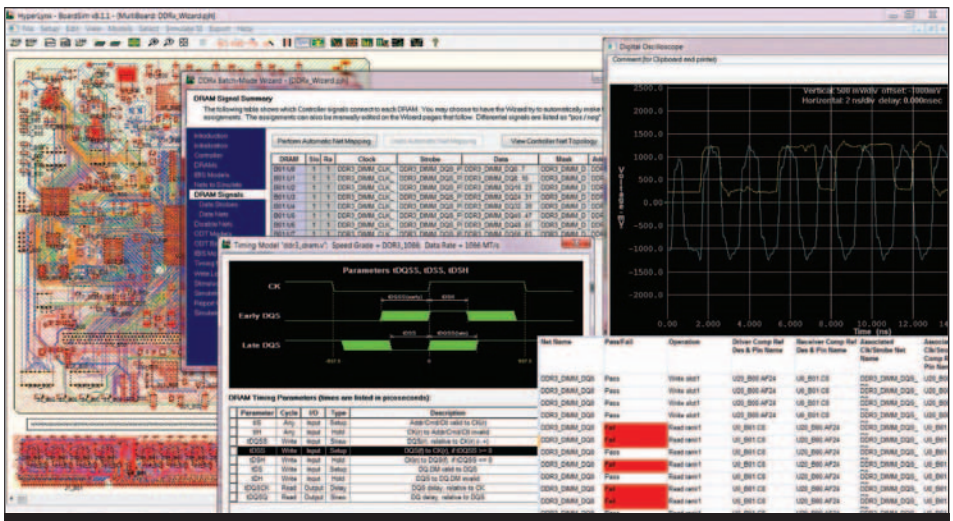

Fig 3: DDR3 bus analysis in HyperLynx DDRx Wizard