Automating analogue design

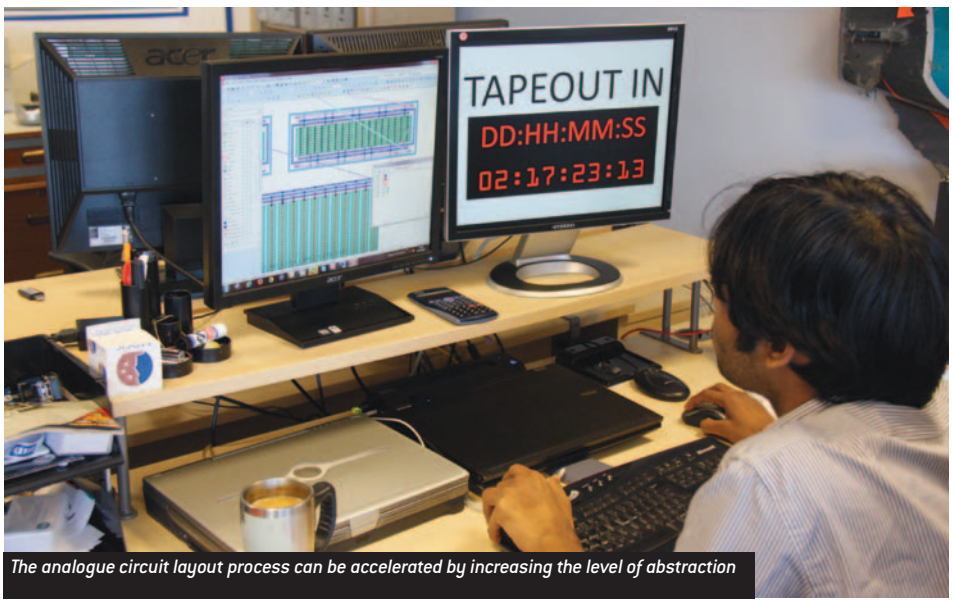
A balanced approach between abstraction and automation matches analogue design requirements. By **Paul Double**.

Despite its continuing – and, in many cases, increasing – importance in modern chips, analogue and mixed signal (AMS) design has proved difficult to automate. While digital design automation has seen rapid advancement during the last 30 years, the only major step forward for AMS designers has been the introduction of foundry verified cells, termed by various eda vendors as T-Cells, PCells, Mcells, Flexcells or Pycells. Beyond this, remarkably little has changed: it is not uncommon to find AMS designers relying on their expertise, experience and 'feel' to perform polygon based layout by hand. But, as design complexity has increased, this approach is becoming increasingly untenable.

In the past, fabrication processes were relatively well characterised and it was possible to check a design against fundamental rules such as metal to metal spacing: established design rule checking (DRC) tools are well suited to this task and the process is relatively efficient. However, design rules for advanced process technology are more complex. Sometimes, designs are simply not DRC checkable. One foundry described the situation thus 'there is no expectation that all recommended rules and practices will be used. Consider each rule and practice. Follow the most important rules and practices whenever possible'. This is hardly a formula for automation.

Absence of automation also produces an unacceptable lack of consistency: each designer effectively works in a 'silo', applying a slightly different set of rules and constraints. The net result is that respins of AMS designs are going up, not down, creating a pressure to standardise and automate.

The eda industry has responded by offering varying degrees of increased automation. Some vendors attempt to inject more parameterisation at the device level. The problem is this does not address the most time consuming element of analogue design (and the element with most impact on quality): layout. A lot of time is still required to generate structures by hand and the quality of the resulting layout varies depending upon the skill of the individual engineer.



The analogue circuit layout process can be accelerated by increasing the level of abstraction

Other providers have attempted to automate the layout process more fully. But this requires a high level approach that may not take full account of the characteristics of the key building blocks or lay them out with the correct considerations. Moreover, the use of global matching rules to the entire layout can have a negative impact. Skilled manual designers understand that a current mirror, for example, should not be laid out in the same way as a differential pair.

None of these approaches can rival the quality of results that can be attained manually. Most also suffer from another fundamental problem; they require the designer to enter a great deal of information, such as circuit design constraints, upfront. As these constraints vary substantially from design to design, this upfront investment of time produces little or no payback.

Layout acceleration

A more effective approach is to accelerate the layout process by increasing the level of abstraction and automation somewhat, without losing the refinement that can be achieved manually. A tool such as Tanner's HiPer DevGen generates 'macro level' cells – reusable design primitives such as differential pairs, current mirrors and resistor dividers –that are often the most time consuming aspect of layout and frequently the parts that are critical to silicon functionality.

The tool applies matching techniques to address common processing artefacts, produces the optimal solution for parasitics and

silicon area and creates devices optimised for high yield. The resulting design primitives are reusable and based only on the manufacturing design rules for the specific technology node. Retargeting the components to another node simply requires the user to input the manufacturing rules for that technology and to regenerate the devices and primitives. So it is possible to move a design quickly to a new technology node or a different foundry.

Because this class of tool stops short of total automation, the layout engineer maintains complete freedom to fine tune the primitives and to place and route them manually.

HiPer DevGen comes with basic default values that meet the requirements of 90% of analogue designs. For example, with a differential pair, it will, by default, attempt to optimise the drain parasitics over the source parasitics. However, with a down mixer, source capacitance is more critical: the designer can change the relevant parameters, regenerate, simulate the design and converge on an optimal design approach.

Reduced design cycle

The overall result is improved layout productivity and reduced design cycle times, at a level of quality that matches that of experienced layout engineers. An example is a classic current mirror circuit (see below).

Double: "Respins of AMS designs are going up, not down."

An experienced layout engineer would be expected to create this structure relatively quickly: however, a poll of such engineers revealed dramatic variations in estimated time to completion, ranging from two hours to two days, with an average time of five hours.

Not only is initial design time unpredictable: the complexity of the design means each engineer would go about it in a slightly different way, introducing potential inconsistencies.

This same complexity also introduces the possibility of a straightforward error that would be time consuming to spot later in the design cycle. In the worst case, the design might be layout vs schematic (LVS) and DRC clean, but have a mismatch: the kind of error that does not show up until silicon is back from the foundry.

A tool such as HiPer DevGen, under control of a layout engineer, can create such a structure instantly. The engineer then floorplans the circuit manually and completes the interconnect. Each device or structure is designed identically and will meet all requirements of the technology, be LVS and DRC clean and have guaranteed matching.

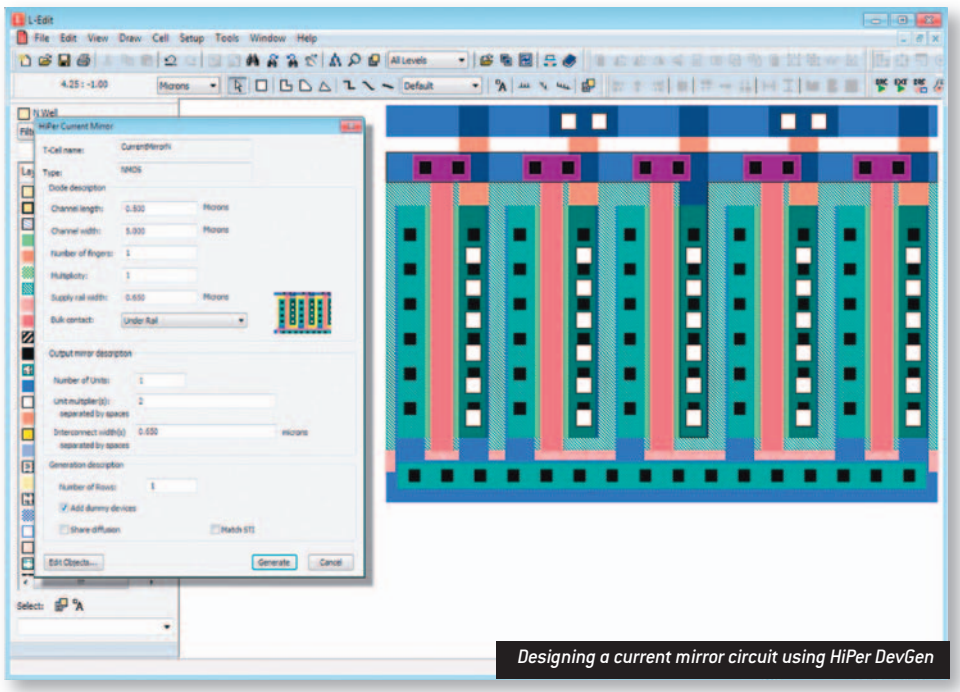
Silicon aware

A further advantage of this level of automation is the generation engine can be made 'silicon aware', supporting design for manufacture (DFM) rules and producing yield optimised devices with special design features such as double contacts and vias.It can account for a number of increasingly important artefacts that are produced by shrinking device geometries. These include the well proximity effect, a phenomenon that causes doping density to vary across the width of an isolation well, which means a transistor's electrical characteristics may vary according to where it is placed within the well and, in particular, if it is placed close to the well edge.

An automated tool can also help designers to account for mechanical stress phenomena, including shallow trench isolation or length of diffusion effects. These effects, which come into play at 130nm and beyond, influence device threshold and mobility, resulting in large potential errors in structures that require matching transistors, like current mirrors.

AMS designers are never likely to get access to the level of automation available to their digital counterparts. But, by focusing on the parts of the flow where they can have most impact, eda vendors are beginning to offer the benefits of consistent quality, predictable time to results and a more natural accommodation of advances in process geometries.

The capabilities of tools such as HiPer DevGen can help designers avoid costly silicon respins and to meet increasingly aggressive time to market demands.



Designing a current mirror circuit using HiPer DevGen

Author profile:

Paul Double is managing director of EDA Solutions (**www.eda-solutions.com**)