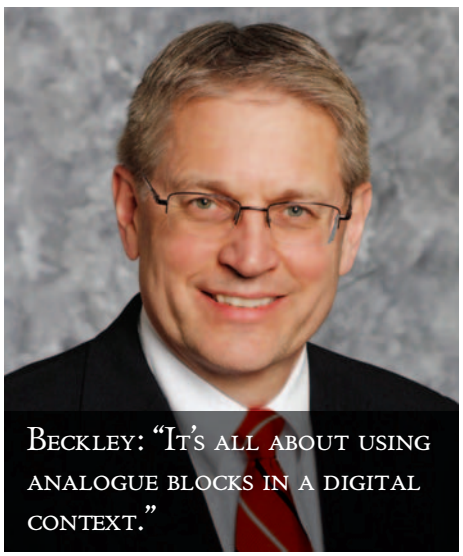
Getting real

How real number modelling is easing the analogue simulation challenge. By **Graham Pitcher**.

The world of electronics brings some interesting conflicts, perhaps none more interesting than the stark contrast between the analogue and digital domains. The technologies are different, the design engineers are different and the ways in which designs are verified are different.

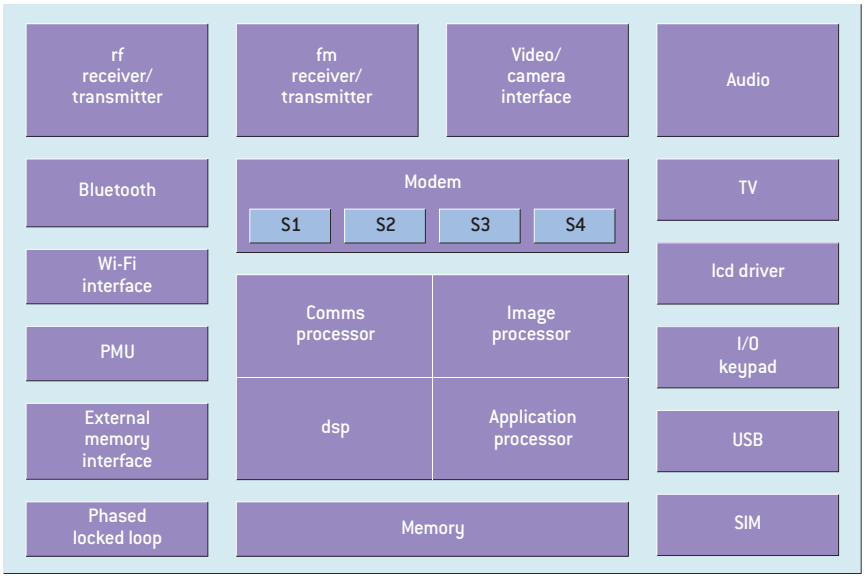
But despite their differences, the analogue and digital domains have to work alongside each other – for example, many consumer products feature large mixed signal chips. There are a number of reasons why this is happening. Tom Beckley, Cadence's senior vp of R&D for custom ic and simulation, explained. "Drivers for mixed signal design include the need for low power consumption, higher bandwidth and technology integration; there's no better example today than Apple products. But, while analogue and mixed signal might seem a straightforward methodology, it's not easy to do."

He highlighted the iPad. "It's full of analogue and mixed signal components; a state of the art mixed signal design with discretes and large devices linked to power supplies and a display.



Beckley: "It's all about using analogue blocks in a digital context."

Fig 1: A generic mixed signal SoC



There's a lot of software and a lot of digital."

Beckley doesn't see things getting any easier. "Over the next five years, mobile data traffic is expected to grow by a factor of 20 and there will be multiple radios to handle the throughput."

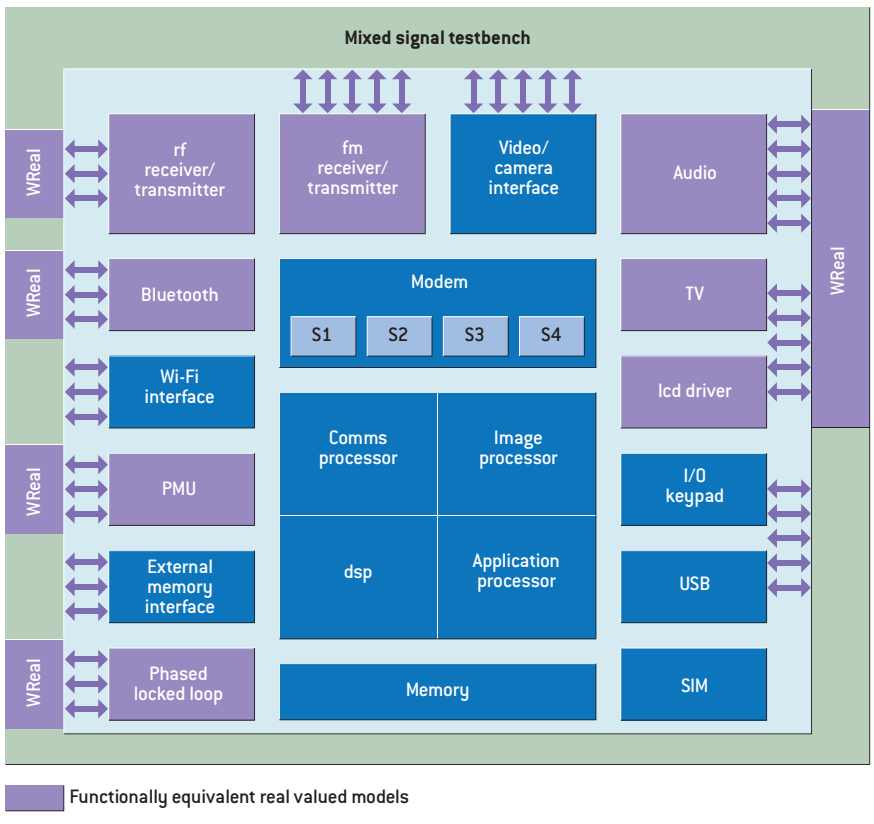
While analogue and mixed signal design is hard enough, verification of those designs is the biggest challenge facing the industry. "Whatever you're designing," Beckley continued, "whether it's a component or a system, you have to make sure there is sufficient verification. But companies don't usually have mixed signal engineers: they have strong analogue and strong digital designers handing off to each other."

Here's the problem: verification of analogue designs is a slow process. Historically, the problem has been addressed through the use of Spice and, more recently, FastSpice. "Everyone wants Spice and FastSpice to get faster," Beckley said, "because it's the classic analogue verification methodology. But Spice isn't sufficient for large analogue designs; it's a bottom up approach and can't handle the level of complexity in today's large designs. The amount of IP and the number of corner cases make verification an overwhelming challenge."

The solution may come from one of those good old electronics contradictions: verifying the performance of analogue blocks in a digital context. And this approach requires the use of a technique called real number modelling. According to Beckley: "Real number models are, in effect, sampled waveforms of the analogue circuit's output."

Analogue and digital simulation differ in the equations they look to solve. Digital solvers handle logical expressions in a sequential manner driven by triggers. Analogue solvers, however, need to solve the whole analogue system matrix at every step. Time values in the

Fig 2: Using real valued models to speed simulation



digital domain are discrete; in the analogue world, they are continuous.

Real number modelling tries to take the best from both worlds. It uses the floating point numbers familiar in the analogue domain, but blends this with discrete time values. This approach offer a level of performance approaching that of a digital simulation, but much faster than the speed of a purely analogue simulation.

John Pierce, a Cadence product marketing director, took up the discussion. "Functional verification is a real problem faced by analogue and mixed signal designers. Take a pll as an example. These used to be simple; driving at one frequency. Today, that pll will support a lot more modes. While it might be easy to add a mode in the digital domain, the number of functional states multiply quickly. An engineer using Spice cannot go through them all."

He said that real number modelling is about using blocks to capture the functional characteristics of an analogue circuit. "It's then about validating the model you have create, making sure it depicts accurately the function of the circuit it represents. It's a representation of analogue functionality, but in the digital world."

Real number modelling also picks up on the concept of assertions. Pierce continued: "We're looking to provide more verification automation into the testbench and one of the ways in which we can do this is by implementing an assertion methodology. A lot of automated tasks in the digital world have been developed from assertions – statements such as 'when this happens, the output pin must be high'."

The benefit of real number modelling can be seen from the example design shown in fig 1. Normally, a large number of blocks would need to be simulated in the analogue domain, a process that would be time consuming. By replacing these with functionally equivalent digital models (purple blocks in fig 2), simulation can be performed in the digital domain, with a significant reduction in the time required.

Beckley noted: "It's all about using analogue blocks in a digital context. If designers don't have a good verification plan, they can end up with a lot of functional errors; and that leads to respins. Errors are usually simple and problems can be solved if you have a good functional plan. With real number modelling, even basic simulators can handle the problems."

The concept of real number modelling is complicated somewhat by another term – wreal, short for real wire in Verilog. The term was developed for use in Verilog-AMS – the analogue and mixed signal implementation of Verilog because the digital version could only resolve logic nets. In effect, it is a datatype that enables analogue accuracy to be achieved in the digital simulation domain.

Pierce explained. "Wreals allow the analogue domain to be represented in the digital world."

In essence, it's a simple concept; in practice, it's not so easy. Designers have access to two kinds of solver: analogue and digital, or logic. "Real number modelling allows analogue functionality to be brought into a logic solver," said Pierce, "and that brings an orders of magnitude increase in performance when running a testbench. If we think about a pll, for example, it might take two days to run a Spice based simulation. If you use the wreal approach, it will only take 10 to 15 minutes."

Beckley backed up the concept in his address to Cadence's CDN Live event, held in Munich in 2012. "Texas Instruments has found a 300 fold increase in verification performance by moving from transistor based simulation to real number modelling."

Texas Instruments isn't the only semiconductor developer to take advantage of the concept. "ARM has used the approach to improve the verification methodology during the design of the Cortex-M0 microcontroller core," said Pierce.

Beckley said that, in general, developers can move away from working at the transistor level to the use of wreal models. "It's an approach that helps to cover all processes and all corners during verification. It's the same testbench, the same environment; you simply 'take out' the transistors, replace them with wreals and get the verification throughput you need."

But Beckley realises that real number modelling is not of much use unless you have good models to start with. "We have been working on ways to make it easier for designers to create the good models they need to represent analogue outputs. Real number modelling has started to take off and we're trying to build bridges between the analogue and digital worlds."