Creating a dynamic solution

Stretching the dynamic range of a/d converters.
By **Robert Fifield**.

Whether your application is focused on wireless communications or instrumentation, the performance bottleneck is often the dynamic range of the a/d converter.

Dynamic range is often a key parameter within signal processing systems and a shortfall can limit the quality and range of signals that can be received. The technical progress made on improving this gateway between the analogue and digital world has not kept pace with Moore's law because the challenges are more fundamental than simply reducing transistor sizes. Methods to increase a/d converter dynamic range are therefore always of interest, although each solution often suits particular applications.

As an example of pushing a/d converter dynamic range beyond what is currently available, the engineers at RFEL were confronted with an application where the customer required an a/d conversion process with a 74dB dynamic range at 800Msample/s. Most commercially available a/d converters capable of sampling at this rate typically offered a dynamic range of 52dB, equivalent to an effective number of bits – or ENOB – of 8.3. ENOB can be calculated as follows:

ENOB = (dynamic range – 1.76)/6.02

This left a shortfall in dynamic range of 22dB; something which had to be resolved in order for the project to be feasible.

Various techniques for extending dynamic range were considered, taking into account their advantages and disadvantages.

• *Increase the sample rate*. The quantisation noise floor of an a/d converter can be reduced by sampling at a higher rate and subsequently band limiting and decimating the output. This has the effect of filtering out-of-band noise sources and, in theory (assuming all noise is incoherent in nature), the dynamic range can be increased by 3dB for each doubling of sample rate. However, at higher sample frequencies, the gains are modest because the ENOB performance of high rate a/d converters also degrades. The cost of the a/d converter should also be considered as this usually increases with sample rate.

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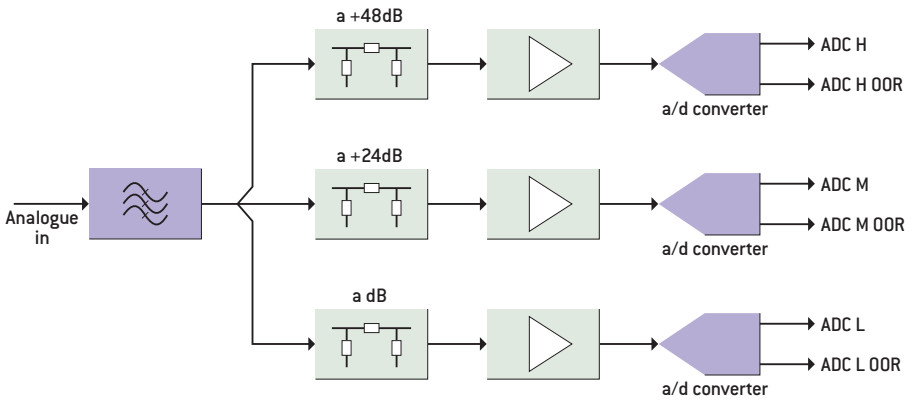
• *Interleaved a/d converters*. A more common solution is to use multiple lower rate a/d converters, which inherently have a better ENOB, to sample the input signal consecutively in an interleaved manner. The dynamic range gains are dependent upon the ENOB improvement of the lower rate converters, which tends to be more significant when targeting high sample rates. To retain any performance gains, careful consideration must be given to amplitude and phase matching between a/d converters. This can involve gain matching, PLL selection and attention to pcb layout. The input bandwidth of the lower rate a/d converters must, of course, be sufficient for the bandwidth of the signal of interest.

• *Non linear gain stage*. If the input signal is passed through a device with a non linear gain, the target dynamic range of the input signal can be mapped onto the available input range of the a/d converter. This effectively produces an a/d converter quantisation step size which increases with the amplitude of the input signal. A disadvantage of this technique is that the signal must be restored by subsequent signal processing, which often requires signal training to guarantee accuracy. Meanwhile, quantisation noise is dominated by the largest part of the signal.

• *Stacked a/d converters*. To make a significant improvement in dynamic range, a stacked a/d converter architecture can be used. In this approach, the signal is split into multiple paths, each with a different gain before input to the a/d converter. If, for example, three a/d converters are used, they would capture large, medium and small signals respectively and the final output would be selected from the most appropriate a/d converter. This approach has an obvious problem; although one signal can be tracked over a large dynamic range, the instantaneous dynamic range – the ability to receive large and small signals at the same time – is degraded. Another potential issue is that each path must be matched carefully to align phase, amplitude and frequency responses.

For the project, the 22dB increase in dynamic range could not be realistically achieved using the first two approaches. The third technique was feasible, but was rejected due to the large quantisation steps for large input signals and the

Fig 1: The stacked a/d converter configuration



overhead of signal training. Further analysis of the system requirements revealed the customer's monitoring application did not require a high instantaneous dynamic range, therefore the feasibility of fourth option was investigated further.

Achieving 74dB of dynamic range requires roughly 12 (74/6) bits. However, the minimum signal to noise ratio (snr) required by the system needs to be added; in this case, approximately 4bit. The total signal range is therefore roughly 16bit. Because phase and amplitude matching is important, identical a/d converters in a dual, triple or quad packaged device would be ideal.

The best option, having considered device cost and performance, was e2v's EV8AQ160, an 8bit quad packaged device. To meet the dynamic range and snr requirements, three of the four packaged a/d converters were used to cover the full 16bit range. The converters were allocated such that the most sensitive – ADC_Low – detected bits 1 to 8. ADC_Mid detected bits 4 to 12 and ADC_High handles bits 8 to 16 (see fig 1). This allows the full 16bit range to be covered, meeting the dynamic range requirement and providing a 4bit overlap to satisfy the snr requirement.

The design and layout of the analogue input network is another potential minefield; particularly because the input signal is split into three different gain paths (see fig 1). To maintain consistent amplitude, phase and frequency response, each path contains an identical active gain stage preceded by a passive attenuator of 0dB, 24dB and 48dB for the high (bits 1 to 8), medium (bits 4 to 12) and low (bits 8 to 16) gain paths respectively. Linear power regulators were used to reduce noise and the high gain signal path was positioned away from other potential sources of noise.

The analogue and digital components were designed, simulated and fabricated onto a 14 layer pcb, allowing multiple bgas to be routed within a small area. The design was tested over the complete signal range under various environmental and emc conditions to ensure robust operation. Figure 2 shows the combined 16bit output for an input signal at full scale (low gain path active) and after it has been attenuated by 76dB (high gain path active). The pulse shape can clearly be observed in both figures. The second figure shows the efforts to mitigate noise have paid off as the system can operate successfully close to the device's quantisation noise floor.

This article has focused upon extending the dynamic range of the a/d conversion process. In the final product, this was the first enabling step before useful information within the input signals could be extracted through digital signal processing. The processing was carried out within multiple high speed fpgas before results were sent out over a network connection.

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Fig 2: Performance at full scale and full scale – 76dB