

Spicing things up

How eda companies are taking analogue design beyond Spice simulation. By **Graham Pitcher**



With the continuing emphasis on digital design, observers could be excused for believing that analogue design had, somehow, 'gone away'. But the real world is different and, as we've said many times before, it's an analogue world.

Mike Demler, a product marketing manager in Synopsys' analogue and mixed signal group, said: "We've been going through a consumer electronics revolution. People say it's a digital revolution, but devices like mobile phones are enabled by analogue electronics."

This enabling technology is often designed at the transistor level. "Because it's targeted at consumer applications," Demler continued, "it has to be cheap and we don't have the luxury of a refined analogue process; analogue and digital often have to work alongside each other on the same chip and analogue circuitry has to work in the presence of digital noise."

Ironically, analogue designers are overcoming these problems by turning to the digital world. "In the old days," Demler recollected, "we may have blown fuses or used laser trimming. Today, because digital is so cheap, we can add a lot of registers because they doesn't take up much space and use them if the circuit is not performing to spec."

Nevertheless, the move to smaller process geometries means analogue

designers are undertaking more complex blocks than ever before. "At this year's ISSCC, for example, papers were describing analogue front ends which run at 5GHz," he continued.

So circuit design techniques are changing. "When you're designing for a 90nm chip, you can adjust transistor size, but you are still limited by the operating voltage, which may be 2.5V, and this means the circuit will be noise sensitive.

"There's also the problems of multiply supply voltages," he continued. "You have to make sure the right transistor is connected to the right supply voltage and you have to do more verification because there are multiple voltages."

Another effect of lower operating voltages is parasitics. "Synopsys is doing quite a bit to help people do circuit level analysis of power and groundplanes, allowing them to find out whether their chip will work," Demler claimed.

Electromigration – an increasingly important phenomenon with smaller feature sizes – causes reliability problems. "You have to be able to measure currents accurately, because faster switching speeds increase current flow and this promotes electromigration."

Demler says these developments have made circuit simulation the most important 'day to day' tool for the analogue designer. Step forward Spice models and their variants.

"Synopsys has been increasing the speed of HSpice, adding more analysis capability to address device reliability and to examine variability – transistors don't match like they used to," Demler noted.

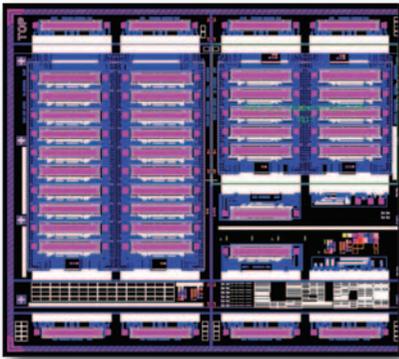
In the latest release of Synopsys' HSpice simulator, multithreading



capabilities speed circuit simulation by taking advantage of multicore computer architectures. As a result, says the company, circuit designers can now run Hspice post layout simulations up to three times faster on single core processors and up to six times faster on four core processors.

Synopsys' HSIM simulator is said to provide better performance than Spice simulation. "Larger circuits can be handled and we've spent time addressing the issue of parasitics."

But Synopsys is not alone in addressing these issues. Electronics Workbench, now part of National Instruments, is equally



concerned with simulation.

NI acquired Electronics Workbench in 2005. "Since then," said Bhavesh Mistry, marketing manager for NI's Electronics Workbench group, which produces the MultiSIM schematic capture and simulation software, "we've been working to improve design quality by improving the component database and by providing links to LabVIEW."

"NI is built on LabVIEW," he continued, "and we have the ability to access real measurements. We're blending real measurements with simulation to give an integrated design flow and believe this will improve design quality before it gets to the prototyping stage."

NI says that, by including simulation in the design process, design errors are reduced and the design cycle is speeded by allowing circuit behaviour to be predicted and better understood. It also allows 'what if' scenarios and provides the ability to optimise key circuits and to

characterise difficult to measure properties.

"A lot of the things we're doing," Mistry continued, "are providing simple links between measurement and simulation. With MultiSIM, all data can link to LabVIEW. If they need to get real measurements into their simulation, they can do it."

MultiSIM is Spice based, but Mistry says it abstracts from Spice so designers can interact with graphical symbols, rather than code. "We're making design as easy as possible," he claimed.

Meanwhile, Tanner EDA has released version 13.0 of Tanner Tools, its Windows based analogue and mixed signal tool suite. The package includes T-Spice, for simulation.

Paul Double is managing director of EDA Solutions, which distributes Tanner EDA products in the UK. "Because Tanner doesn't have the development budget of the big companies, it has to pick and choose what to do in the most efficient manner possible. For instance, the latest release adds Verilog-A model support to

users are developing technology using 0.18µm technology and older. We're seeing more and more customers taking a step back," he claimed.

The Active Matrix Systems (AMS) Group at Philips Research Labs in Redhill started using the Tanner EDA tool suite a year ago and has completed its first two mixed signal ic designs using the tools (see inset picture on this page). The AMS group specialises in analogue and mixed signal ic designs with up to 100,000 transistors.

Steven Deane, AMS group project manager, said the team was impressed with the tools' functionality and ease of use. "Schematics and design data



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Mike Demler, Synopsys

T-Spice, but we've bought in tried and tested software from Tiburon Design Automation. This approach helps us meet customer requirements in a timely fashion without spending a lot of money." The company has also partnered with the Technical University of Delft to add a parasitic extraction tool to the package.

In Double's opinion, version 13 features functionality 'for which you would previously have had to go to Mentor and Cadence'. "Tanner's aim is to provide 80% of the functionality (offered by Mentor and Cadence) for 20% of the price and the company is looking to move that to 90:10."

He sees the 'big boys' putting up their prices and 'following the bleeding edge'. "Most of our customers and most European

imported from other tools was instantly readable and usable. Simulation was comparatively easy to set up and we were happy with the functionality of the layout tools, especially the design rule checkers."

The team also found unexpected benefits with the pc based tools, compared to the workstation hosted suite it had used previously. For instance, the tools enabled a more flexible workflow and greater mobility.

Double believes this is the start of a bigger migration. "We are seeing a lot of big company customers coming to us because they are seeing their bills going up disproportionately to what they are getting," he concluded. ■