Embedded dram and sram have long provided an effective means to address different performance and functional requirements for on chip storage. However, the memory content of SoCs now accounts for the largest proportion of the die area and an increasing number of designs demand more from a memory – or at least higher density – than the current crop of technologies can provide.

There is considerable impetus behind the development of new forms of embedded memory. The 2003 edition of the International Technology Roadmap for Semiconductors (ITRS) identifies a number of candidates being groomed for the sub 100nm SoC of the future, including magnetic ram, phase change memory and molecular memories. Unfortunately, the promise of such techniques rests with the hope of integrating new and exotic materials into the baseline cmos process. In addition, these memories use multi device cell structures (one transistor plus one other device), which are often difficult to scale to smaller geometries.

Embedded dram is frequently employed in designs requiring high density memory storage and high performance logic on the same chip. However, it adds a premium to the cost of an SoC, typically 25% with single transistor, single capacitor (1T/1C) cell technologies. The additional cost comes from the extra mask steps required to fabricate these capacitor elements, which rely on complex stacked or trench silicon device structures. More urgently, the reluctance of these capacitor elements to scale effectively beyond the 90nm node looks likely to become a major obstacle to future die size reductions.

A number of capacitor less dram technologies have been explored over the years. However, these have largely introduced additional compromises of one kind or another. The cell design of the two transistor capacitor less dram (abbreviated to 2T cdram), for example, operates with an additional transistor and four signal lines, thus failing to answer the call for a denser cell structure.

Exploiting SOI effects
A novel single transistor (1T) dram concept is the ‘floating body’ dram. The technique takes its name from the floating body effects that arise within mosfets fabricated using silicon on insulator (SOI) processes. These effects, characterised by an accumulation of charge within the body of the device during operation, have long been considered a nuisance to device developers using SOI.

However, on an SOI process, 1T dram cells can actively exploit the floating body effect, permitting the use of a single transistor cell structure which only requires three signal lines to operate.

“Speed improvements are a natural by product of using a higher density memory technology with shorter wire lengths.”

Mark Eric Jones, Innovative Silicon
SOI process technology is gaining ground in more advanced SoC designs and offers a number of benefits over bulk CMOS, including improvements of roughly 35% in either speed or power consumption. It also provides better RF and mixed signal performance, as well as a greater level of immunity to radiation.

SOI, however, is 10 to 15% more expensive than bulk CMOS. But the use of floating body DRAMs on SOI chips can offset these costs in designs where a sufficiently large proportion of the chip is occupied by memory. This technology has been developed by Innovative Silicon (ISi) as Z-RAM – or zero capacitor DRAM. ISi is the first company to demonstrate working floating body memories and, so far, Z-RAM bitcells have been demonstrated at nine different foundries and megabit size test chips have been produced on 90nm wafers.

In a standard 90nm SOI logic process, the Z-RAM bitcell size can be optimised down to approximately 0.10µm² (or 12F² - where F is the minimum feature size), one tenth of the size of the smallest SRAM bit cells. Even ISi’s first 90nm Z-RAM designs, with bit cells of 0.18µm², were smaller than embedded DRAM bit cells on the 90nm node without needing the additional masks and processing steps that embedded DRAM demands.

In a chip design where 70% of the die area is taken up by memory, the use of Z-RAM instead of embedded SRAM can yield die area savings of around 55%. For a chip that would otherwise have used bulk CMOS, the cost premium associated with the use of SOI offsets these gains, but still results in a net die cost saving of at least 40% due to the improved yield of the smaller resulting die.

For an nmos device, the bit cell stores a ‘1’ by applying a positive pulse voltage to the drain of the transistor (see figure 1). This, in turn, causes an excess of positive charge to accumulate in the body of the device, created by a mechanism called ‘impact ionisation’. The effect sets up an increase in the channel current, IDS, which can be measured as a logic 1 value.

A ‘0’ can be stored in the cell either by applying a positive pulse voltage at the drain or gate, or by applying a negative voltage pulse to the drain. The result is a build up of excess negative charge in the device body and a reduction in the current flowing through the channel, measurable as a logic 0.

Taking its pulse

The cell is read by applying a pulse to the selected transistor bit cell and using a current mode sense amplifier to compare the resultant current level in the channel to the current flowing through a reference cell.

A further improvement can be made in the cell area by sharing contacts between the source and drain of the transistor. The result is a grid like chip layout comprising rows of adjacent crosstreeing signal lines. The cell uses a word line (WL) to bias the device gate, a bit line (BL) to connect the drain, and a source line (SL) to connect the cell to ground (see figure 2).

This small bit cell size, together with a lithography friendly array bit line and word line structure, results in an overall density capability of between 0.30 and 0.4mm² per Mbit of embedded Z-RAM on the 90nm node. More, the simplicity of the bit cell layout (and the lack of capacitive element) permits Z-RAM technology to scale well to at least the 22nm process node – ISi has already measured suitable characteristics in the FinFET transistors that may well be used at that time.

Speed improvements are a natural by product of using a higher density memory technology with shorter wire lengths. The Z-RAM can read or write in less than 3ns – much faster than embedded DRAM. Furthermore, the power consumed by read or write operations is 30% less than with embedded DRAM.

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