White Paper

Tradeoffs of LDO Architectures and the Advantages of Advanced Architecture "Capless" LDOs

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ABSTRACT

Power management of battery-powered electronic devices is becoming increasingly more important for the present and future microelectronics industry. This application note details the difference between low dropout (LDO) voltage regulators that use output capacitance and those that do not and how your system designs can benefit from or be improved by not using an output capacitor.

Capless LDO voltage regulators improve system efficiency, subsequently prolonging battery life of the device, while simultaneously reducing your overall costs.

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Table of Contents

INTRODUCTION

The demand for higher performance and more efficient battery-powered electronic devices is continuing to increase, driving designers to design electronic systems that consume minimal power while providing best-in-class dynamic performance. Subsequently, the power management of such devices is increasingly more important for the present and future microelectronics industry. To be successful, it is vital to increase the operating life of the device and the battery while reducing the total system cost.

Large systems are divided to provide isolation, interference, and cross talking. As a consequence, an increasing number of voltage regulators that supply the different subsystems are required. In particular, the low dropout (LDO) voltage regulator is often used to provide low voltage, low noise, and accurate output voltage. These regulators can be used as standalone products, to provide a stable, highly accurate, and noise-free voltage to a load in a bigger system, or as an embedded architecture within a system on a chip (SoC), to provide local, noise-immune voltage regulation to power the latest ASIC or CPU architectures. A typical LDO regulator normally requires an external capacitor, in the range of a few microfarads. This external capacitor is usually bulky but necessary to significantly improve the transient response, power supply noise rejection (PSR), and stability of the LDO. On the other hand, the external capacitor increases the IC pin count in SoC applications, occupies valuable board space, and degrades reliability. Additionally, commercial LDOs with external capacitors require the capacitor non-idealities to be bounded, severely constraining system-on-chip (SoC) solutions.

SELECTION OF LOW DROPOUT LINEAR VOLTAGE REGULATORS

There are many applications for LDOs and their corresponding specifications are varied. One critical parameter is quiescent current (IQ). Having minimal operating and shutdown currents will increase operating time in battery-operated electronics. IQ is only one of many parameters. LDOs used for mobile and battery-powered devices must also provide a noise-free supply voltage. Other important parameters are low dropout voltage, fast settling time, and light load- and low line-regulation. Economic and robust LDOs are important in a variety of applications.

In the last decade, there has been a big push to yield cheaper LDOs with improved reliability. A conventional LDO consists of a voltage reference, an error amplifier, a resistor feedback, a pass

transistor, and an external load capacitance (CL). Some recent trends focus on developing LDOs without external load capacitance. These are referred to as capacitor less, capless, and capacitor-free. The absence of the external capacitor brings many economic advantages; however, significant degradation can often be seen in areas of transient performance and power supply noise rejection (PSR). As a result, significant design challenges accompany the capacitor-free LDO that must be economically and efficiently overcome. Key design issues for LDOs are presented below.

LOW DROPOUT LINEAR (LDO) WITH OFF-CHIP LOAD CAPACITOR

Traditional LDOs use off-chip output capacitors because the topology has one dominant pole at the output, which yields good stability, as well as reasonable power supply rejection (PSR), and load line regulation. LDOs use three main types of capacitors: ceramic, tantalum, and in some larger power applications, aluminum electrolytic. Ceramic capacitors are the most common capacitors used in LDO applications for their low cost and reduced footprint size. These external, discrete capacitors can have critical non-idealities, which mainly consist of a parasitic effective series resistance (ESR) and an effective series inductance (ESL). This inductance restricts the capacitor's performance at high frequency. For this reason, it is common, when electrolytic or tantalum capacitors are employed, to add a small ceramic capacitor in parallel to allow bypassing of the electrolytic/ tantalum capacitance, thus extending the useful frequency range of the external capacitance.

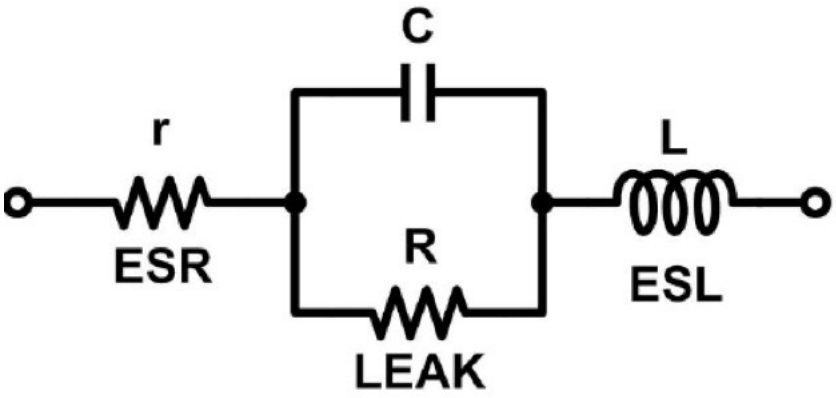
The smaller the ESR, the better the performance; however, if the impedance of the output capacitance is too small, the dynamic response can be degraded, as this becomes a dominant pole that can dramatically reduce phase margin. On the other end of the spectrum, a large ESR can create a zero that extends the unity gain frequency in the closed loop, yielding a larger unity gain frequency but severely deteriorating the phase margin, making the system unstable. We should also keep in mind that these capacitor non-idealities are sensitive to mechanical effects, and vary with bias and temperature. For ceramic capacitors, the ESR is in the range of several 10s of milliohms and in the case of tantalum caps, 100s of milliohms. Therefore, different capacitor technologies have different performance targets and cost.

There are other considerations that should be taken into account when selecting the output capacitor besides the ESR. For example, in cases of failure, ceramic capacitors behave as an open circuit, while tantalum capacitors fail shorted. In addition, ESR of tantalum capacitors are

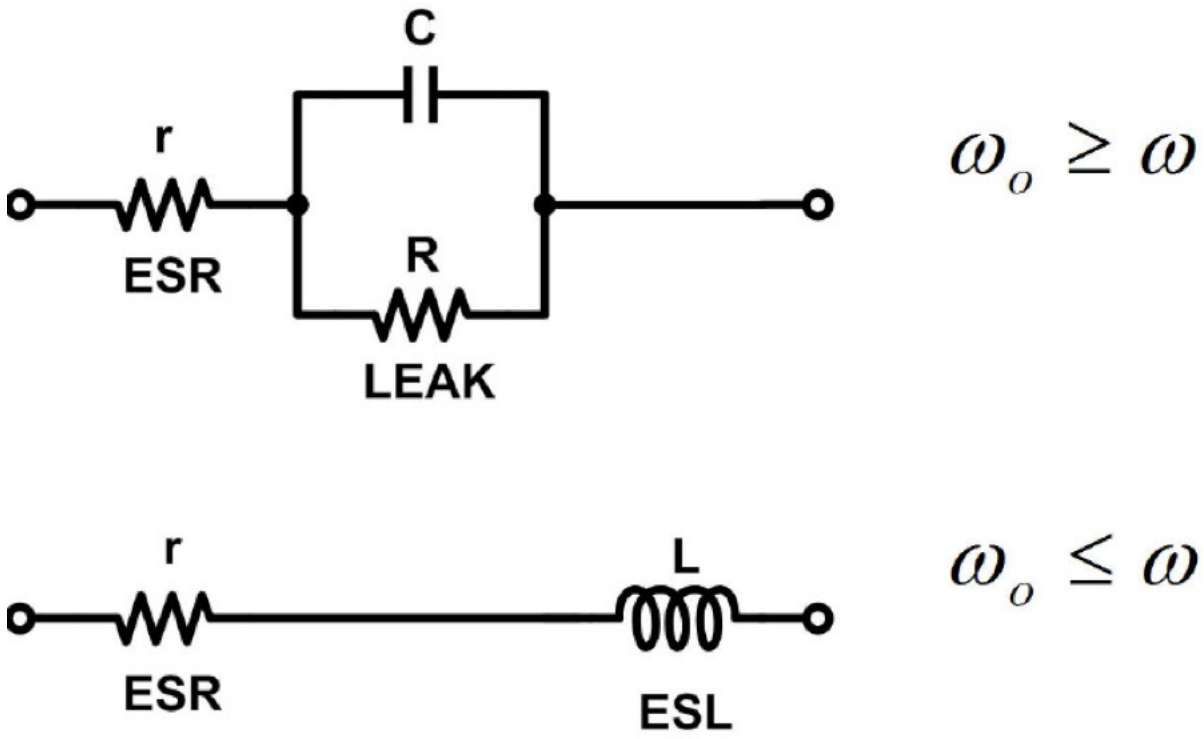
more sensitive to temperature variations, forcing designers to anticipate how to compensate for this perturbation. It is helpful to remember that Gain and Phase margin minimums in loop stability analysis are there to protect against the various shifting parameters, like capacitance over temperature, which can be +/- 20% or more. Because ESL and ESR are not specified vs temperature or given a target tolerance, they can vary widely, causing their impact over temperature on loop dynamics to be extreme.

In practice, many LDO applications often require the addition of external capacitors at the output and input of the LDO. Having a stable LDO for any output capacitor value is not a trivial design specification to meet, since the majority of commercial LDOs can only guarantee stability for a specific output capacitor range. To satisfy stability, LDO manufacturers impose restrictions on the ESR of the output capacitance, requiring it to be within a specific range of values. It's the maximum ESR that is the critical value yielding a reasonable phase margin to ensure a stable operating LDO.

An external capacitor model is shown in Figure 1. It consists of four impedances, connected as shown. The first impedance is the ESR, the second is the ideal capacitor connected in parallel with a large leakage resistor, and the last impedance is an inductor ESL. There exist several elaborate models of a real capacitor; here we include a relatively simple model of a real capacitor to illustrate its nature. The behavior of this model for low and high frequencies related to the resonance frequency ωo is also illustrated. It can be seen that it is mainly a function of the capacitor C and the ESL.



$$\omega_o^2 = \frac{r+R}{R \cdot L \cdot C}$$



Figures 1. External Capacitor Model

It should be noted that an incorrect selection of the external load capacitor might lead to stability problems, excessive power dissipation, and noise, which will all reduce the battery and product life. There are often real, practical situations where the input capacitance of the device to be powered by the LDO is not known in advance. In such cases, LDOs are required to properly operate with capacitance loads from 0 to a few microfarads. This is why we should explore the use of capless LDOs and their advantages and limitations.

CAPACITOR-FREE LOW DROPOUT (LDO)

The absence of the external load capacitance is extremely attractive due to the fact that this absence can translate into a reduced PCB area and lower BOM costs. Additionally, one less capacitor is one less device that can fail and does not need to be soldered. In SoC applications, the savings and benefits are even greater due to the reduction of external pins as well as pad and package connections, and their associated cost and impedance. Eliminating the external capacitor also brings elimination of the PCB traces, some metal paths, and bond wires. In addition, the severe non-idealities of the discrete capacitors such as ESR and ESL are eliminated. Usually, many LDOs

are used in complex systems; therefore, not using external capacitors has a multiplier effect on these benefits. Figure 2 below depicts the differences between the capacitor-free and the off-chip capacitors LDOs.

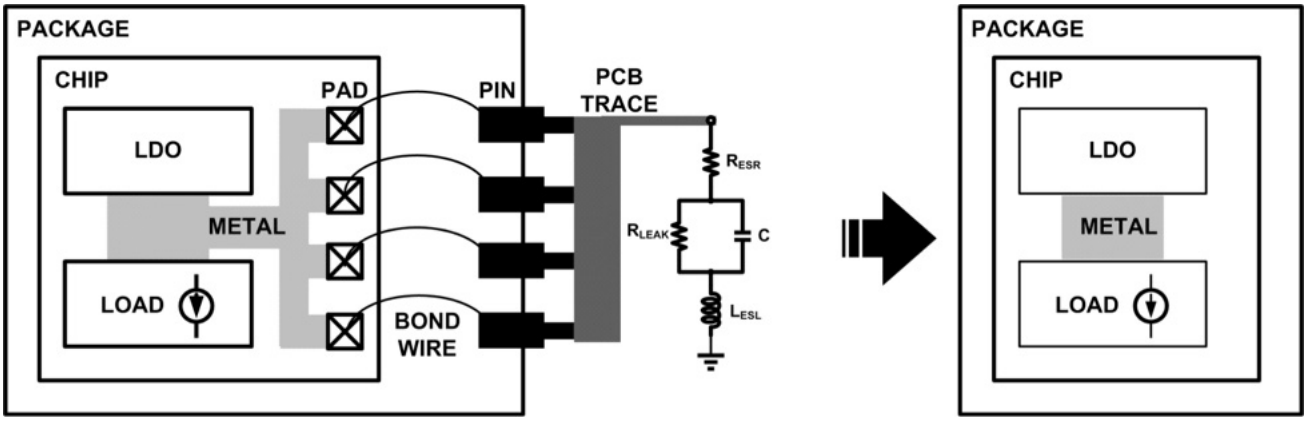


Figure 2. Off-Chip Capacitor LDO versus Capacitor-Free LDO

The capacitor-free LDO is appealing for both SoC and discrete applications. The conventional off-chip capacitor LDO depends heavily on its stability and high performance on the off-chip capacitor. This off-chip capacitor LDO has a dominant pole at the output node and can be designed to be stable for certain capacitor and specific maximum ESR and ESL. The capless LDO doesn't have an output dominant pole but an internal dominant pole varying with the load current. Providing a stable LDO under any load current load range and a load capacitor range from no capacitor up to a few microfarads is a challenging design problem. Literature shows that a number of solutions have been proposed for capless LDOs, but they are functional under only a limited output current and/or a maximum load capacitance. Keep in mind that there are applications where the capacitance load presented to the LDO can be extremely low, but other applications can present capacitance of the order of a few microfarads. The capless LDO must be stable under all of those extreme scenarios.

CONCLUSION

In this paper, we have presented the advantages of capless LDO architectures. As previously mentioned, capless LDO architectures provide SoC or system designers with several advantages in terms of cost and board area savings. There have been attempts in the academic world and the industrial sector to provide a practical capless LDO, but many of the capless LDO architectures available today have severe limitations, preventing their practical use. Several capless LDOs

reported in today's literature obtain decent results, but only for a specific parameter such as load regulation, line regulation, or settling time. The large majority can only guarantee stability for an external load capacitance between 0 pfd to 100 pfd and a maximum load current of less than 100 mA and suffer significant losses in areas of dynamic performance and PSR effectiveness.

There is, however, one capless LDO architecture existing in the market today that provides true capless operation as well as low quiescent current, low dropout voltage, better than 1% output voltage accuracy, >40dB power supply noise rejection (PSR) at 10MHz, and best-in-class dynamic load and line transient performance all while providing unconditional stability regardless of the capacitance of the load.

Vidatronic, Inc has developed an advanced architecture capless LDO that is unconditionally stable, with or without output capacitance up to 4.7uF. Using their patent-pending Noise Quencher™ technology, Vidatronic LDOs are able to obtain best-in-industry transient performance and PSR, all without using output capacitance. These advantages make this family of LDOs the optimum choice for SoC and system designers alike. For more information on Vidatronic's advanced architecture LDO's, power switches, and voltage references & regulators, go to www.vidatronic.com/ip-solutions.

For more information, please visit vidatronic.com

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